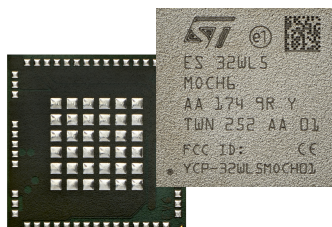


Multiprotocol LPWAN dual-core module 32-bit Arm® Cortex®-M4/M0+ LoRa®, (G)FSK, (G)MSK, BPSK



LGA92 (10x10 mm)
Non-contractual images

Product status link

[STM32WL5MOC](#)

Features

Includes ST state-of-the-art patented technology.

Integration of STM32WL55JC:

- Dual-core Arm® Cortex®-M0 and Arm® Cortex®-M4 CPU
- ART Accelerator with a speed of up to 48 MHz
- 256-Kbyte flash memory
- 64- Kbyte SRAM with sub-GHz radio transceiver
- Embedded 32 MHz radio TCXO and 32 kHz RTC crystals
- All RF components for transmission and reception matching network, including default antenna filter
- STSAFE-A110 footprint
- Metal shield coating

Supporting:

- Frequencies from 864 MHz to 928 MHz
- Compatible with standardized or proprietary protocols such as LoRaWAN®, Sigfox™, or W- MBus (fully open wireless system-on-chip mioty).
- Compliant with radio frequency regulations such as ETSI EN 300 220, FCC CFR 47 Part 15, and Japanese ARIB STD- T-108
- Rx sensitivity: –123 dBm for 2-FSK (at 1.2 Kbit/s), –148 dBm for LoRa® (at 10.4 kHz, spreading factor 12)
- Transmitter high output power, programmable up to +22 dBm
- Transmitter low output power, programmable up to +15 dBm
- 37 GPIOs

Hardware configurations (2-layer PCB compatible)

- Transmitter high-output power programmable up to 22 dBm
- Transmitter low-output power programmable up to 15 dBm
- Transmitter high- or low-output power capable with external switch control

Ultra-low-power platform

- 1.8 V to 3.6 V V_{DD} voltage range
- –40°C to 85°C temperature range
- Embedded SMPS

10x10 small form factor

All packages are ECOPACK2 compliant

1 Introduction

This document provides information on STM32WL5MOC modules, such as description, functional overview, pin assignment and definition, electrical characteristics, packaging and ordering information.

For further details on the STM32WL55 module, refer to the dedicated product datasheet (DS13293) and reference manual (RM0453).

This document should be read with the multiprotocol LPWAN dual core 32-bit Arm®Cortex®-M4/M0+ LoRa®, (G)FSK, (G)MSK, BPSK, up to 256KB flash, 64KB SRAM datasheet (DS13293) and the STM32WL5x advanced Arm®-based 32-bit MCUs with sub-GHz radio solution reference manual (RM0453). Both documents are available from the STMicroelectronics website .

For information on the Arm® Cortex®-M4 and Arm® Cortex®-M0+ cores, refer respectively to the Cortex®-M4 technical reference manual and to the Cortex®-M0+ technical reference manual, available from the www.arm.com website.

For information on LoRa® modulation, refer to the Semtech website. (<https://www.semtech.com/technology/lora>).

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.



2 Description

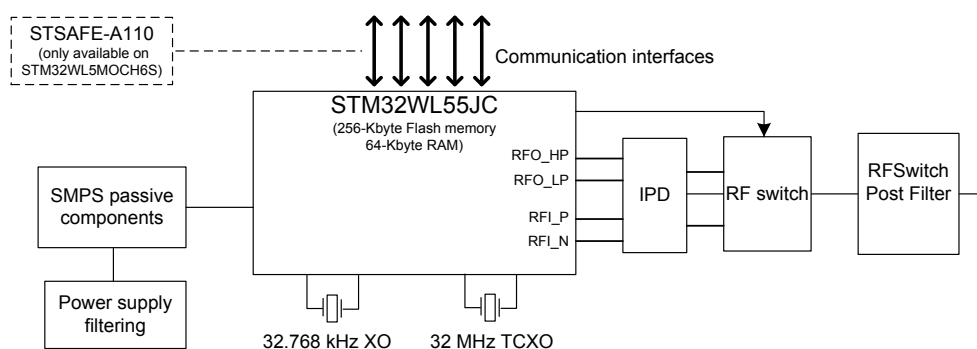
The STM32WL5MOC long-range wireless and ultralow-power certified module embeds a powerful and ultralow-power LPWAN-compliant radio solution, enabling the following modulations: LoRa®, (G)FSK, (G)MSK, and BPSK. The STM32WL5MOC does not require any RF expertise. It is the best way to speed up any development, and to reduce associated costs. This module is completely protocol stack royalty-free.

Table 1. STM32WL5MOC features and peripheral counts

| Feature | | STM32WL5MOC |
|-------------------------------|--|-------------------------------|
| CPU | | Arm®Cortex®-M4 and Cortex®-M0 |
| Maximum CPU frequency (MHz) | | 48 |
| Flash memory density (Kbytes) | | 256 |
| SRAM density (Kbytes) | SRAM1 | 32 |
| | SRAM2 | 32 |
| Radio | LoRa | yes |
| | (G)FSK | |
| | (G)MSK | |
| | BPSK | |
| Radio PA | Low output power (up to 15 dBm) | yes |
| | High output power (up to 22 dBm) | |
| Timer | General purpose | 4 |
| | Low power | 3 |
| | SysTick | 1 |
| Communication interface | SPI/I2S | 2 (1 supporting I2S) |
| | I2C | 3 |
| | USART | 2 |
| | LPUART | 1 |
| Watchdog | Independent | 1 |
| | Window | 1 |
| RTC (with wake-up counter) | | 1 |
| DMA (7 channels) | | 2 |
| Mailbox and semaphores | | 1 |
| Security | AES 256 bits | 1 |
| | RNG | 1 |
| | PKA | 1 |
| | PCROP, RDP, WRP | 1 |
| | CRC | 1 |
| | 64-bit UID compliant with IEEE 802-2001 standard | 1 |
| | 96-bit die ID | 1 |
| | Storage and management of secure keys | 1 |
| | Secure sub-GHz MAC layer | 1 |

| Feature | | STM32WL5MOC |
|-------------------------------------|-------------------------|--|
| Security | Secure firmware update | 1 |
| | Secure firmware install | 1 |
| Tamper pins | | 3 |
| Wake-up pins | | 3 |
| GPIOs | | 37 (35 on STM32WL5MOCH6S) |
| ADC (number of channels, ext + int) | | 1 (12+4) |
| DAC (number of channels) | | 1 (1) |
| Internal VREFBUF | | Yes |
| Analog comparator | | 2 |
| Operating voltage | | 1.8 to 3.6 V |
| Ambient operating temperature | | –40 to +85 °C |
| Package | | LGA92 (10x10 mm) |
| STSAFE-A110 | | Available on STM32WL5MOCH6S part numbers. Not available on STM32WL5MOCH6 part numbers. |

Figure 1. STM32WL5MOC block diagram



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3 Functional overview

The module is an SIP LGA92 package (system in package land grid array) that integrates the STM32WL55JC microcontroller (MCU).

The STM32WL5MOC includes the following components:

- LSE 32 kHz XO (crystal oscillator).
- HSE 32 MHz TCXO (temperature compensated crystal oscillator).
- An IPD (integrated passive device), integrating matching network for transmission output to matching network.
- Passive components for SMPS.
- An antenna matching.
- STSAFE-A110 footprint.

Note: For more information on the STSAFE option, contact the local STMicroelectronics sales office.

3.1 Power supply

Power supply requirements are identical to a regular STM32WL55 MCU. Refer to the product datasheet (DS13293).

Filtering capacitors on power-supply pins and components for the SMPS are already integrated into the module.

3.2 SMPS

The SMPS passive components are fitted in the module (see the reference manual and application notes for recommendations on how to use the SMPS).

3.3 Clocks

As the module integrates a 32.768 kHz crystal for LSE, and a 32 MHz crystal for HSE, it is not possible to use any clock in bypass mode.

- The LSE must be used in high-driving capability: `RCC_BDCR_LSEDRV[1:0] = 11` (see the reference manual for more details).
- The HSE does not need any tuning or calibration as a TCXO is used.
- LSCO and MCO outputs are available.

3.4 RF antenna impact

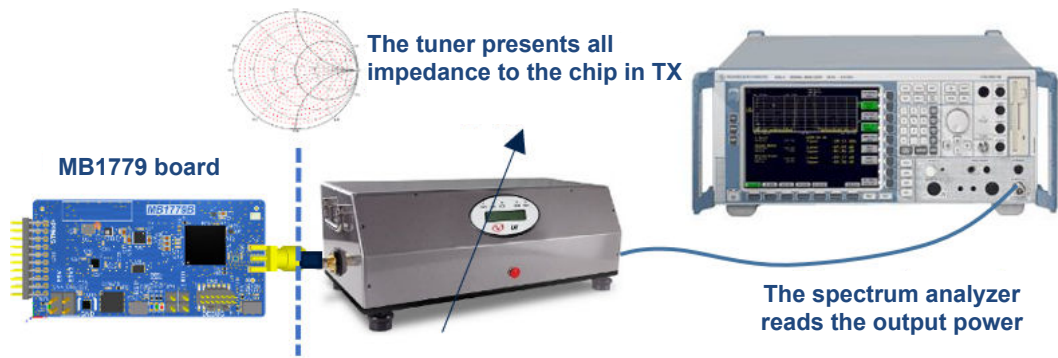
The module can be connected to different antenna types. However, depending on the impedance seen by the module, the RF performance (Tx or Rx) may be impacted.

This section details the limitations obtained by load pull and source pull measurements on the MB1779 (CEB) board.

3.4.1 Impact of the antenna choice on the Tx performances

Load pull setup

Figure 2. Load pull setup

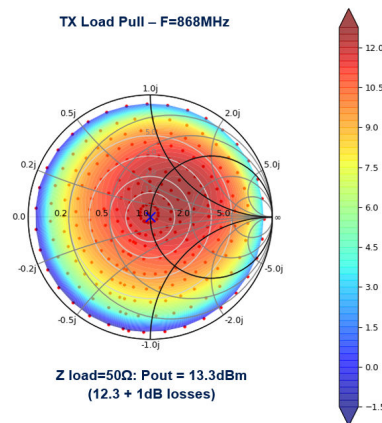


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Note: Loss coming from both the tuner and the cable is estimated at 1dB.

Limitations obtained in Low power mode at 868 MHz

Figure 3. Limitations in Low power mode at 868 MHz

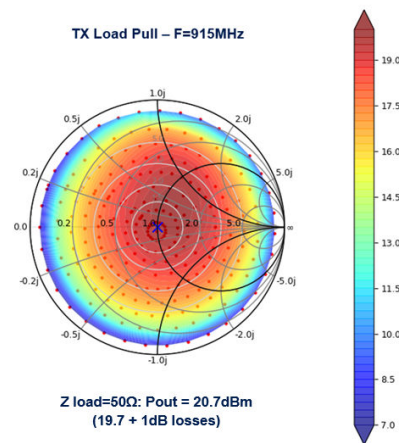


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- To keep an output power > 13 dBm, the TOS presented to the module should be ≤ 2 .
- The maximum output power (13.7 dBm) is obtained for Z load = $62 + j \times 30$.

Limitations obtained in High power mode at 915 MHz:

Figure 4. Limitations in High power mode at 915 MHz

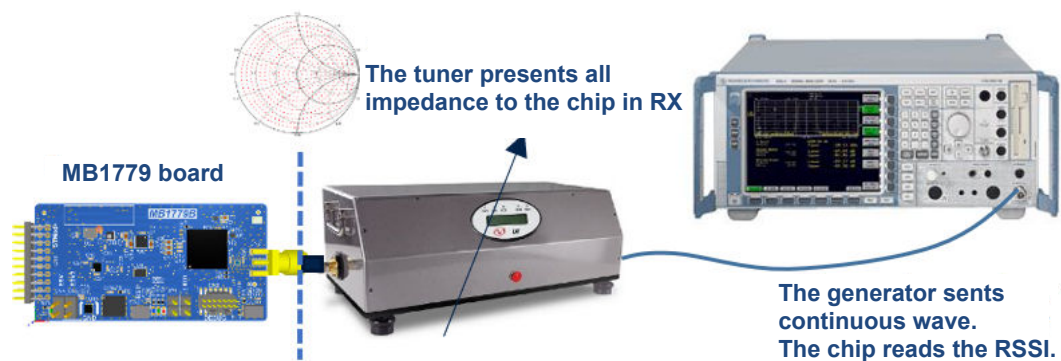


- To keep an output power > 20 dBm, the TOS presented to the module should be ≤ 2 .
- Max output power 21 dBm is obtained for $Z \text{ load} = 63 + j \times 22$.

3.4.2 Impact of the antenna choice on the Rx performances

Source pull setup

Figure 5. Source pull setup



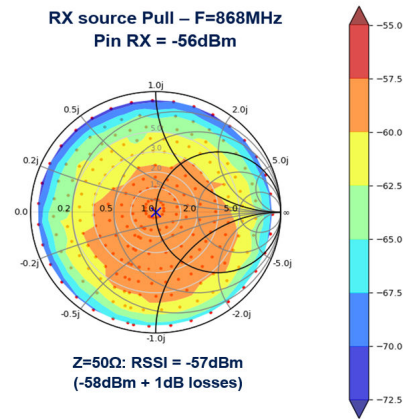
Note: Loss coming from both the tuner and the cable is estimated at 1 dB.

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Limitations obtained at 868 MHz

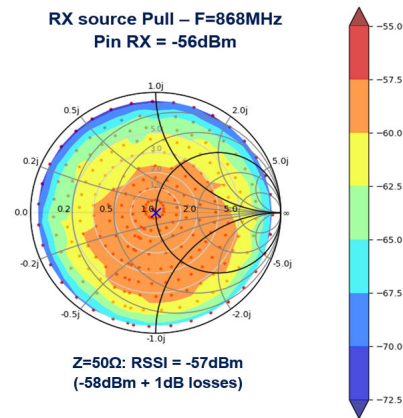
Figure 6. Limitations obtained at 868 MHz



- To keep a correct RSSI, the TOS presented to the module should be ≤ 2 .

Limitations obtained at 915 MHz

Figure 7. Limitations obtained at 915 MHz



- To keep a correct RSSI, the TOS presented to the module should be ≤ 2 .
- To keep good RF performances for both Tx and Rx, the TOS of the antenna should be ≤ 2 .

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3.5 Hardware configurations

3.5.1 Solder bridge vs DC switch configuration

Figure 8. Solder bridge configuration

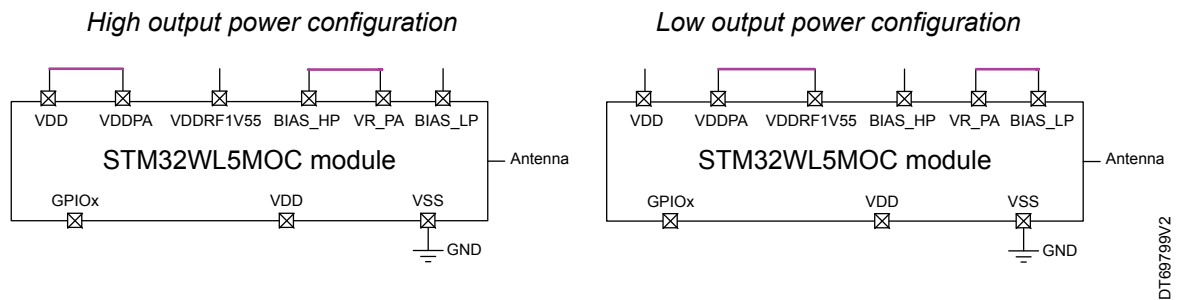
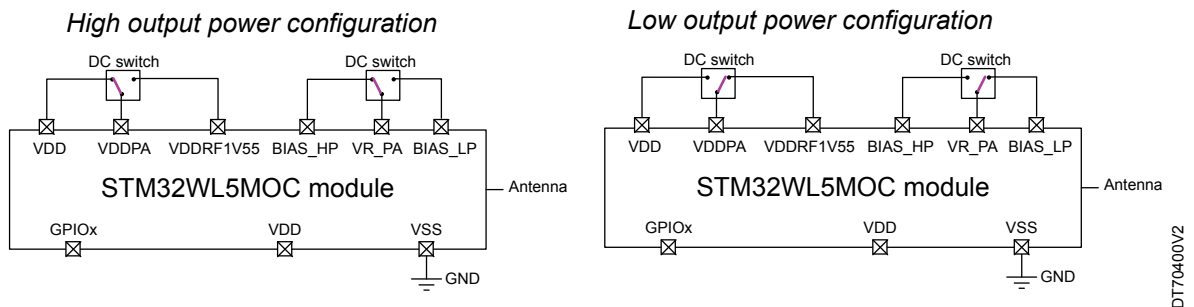


Figure 9. DC switch configuration



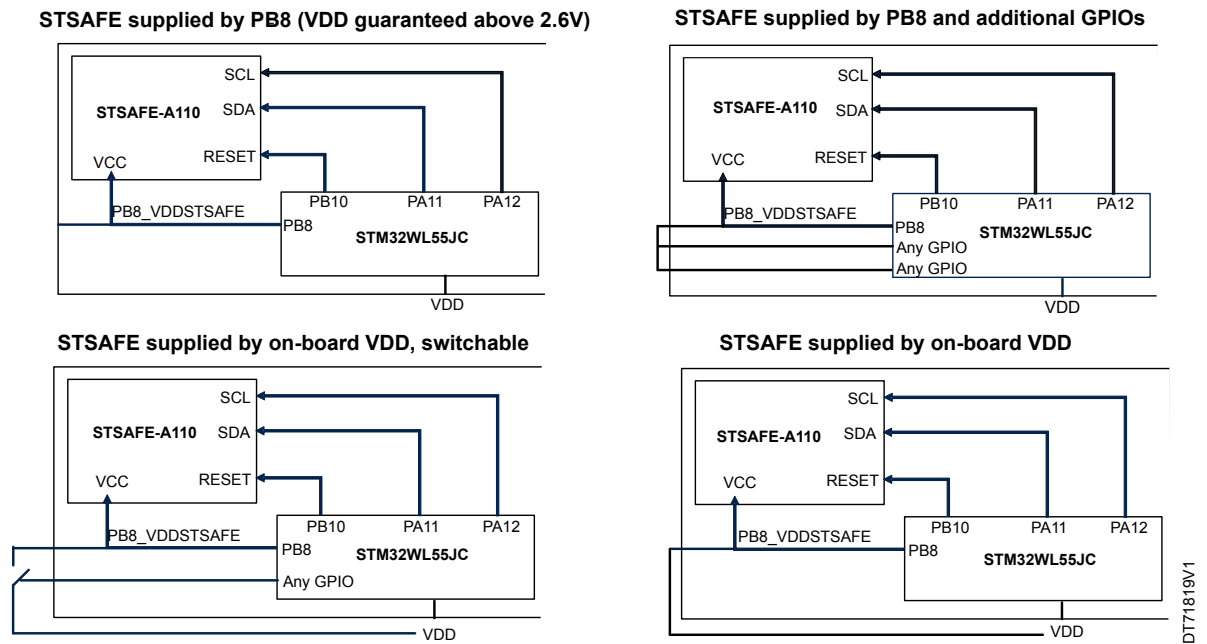
3.5.2 STSAFE supply

STSAFE is integrated in STM32WL5MOCH6S. To optimize power consumption, in particular in low-power mode, the GPIO PB8 controls the STSAFE supply.

When STSAFE needs to be used, GPIO PB8 must then be set up in an output configuration, and forced to '1'. STSAFE can sink up to 21 mA of power consumption. Using only PB8 as a supply limits VDD to a voltage ranging from 2.6 V to 3.6 V. See the schema "STSAFE supplied by PB8 (VDD guaranteed above 2.6 V)".

To support the full voltage range (1.8 V to 3.6 V), different options are available:

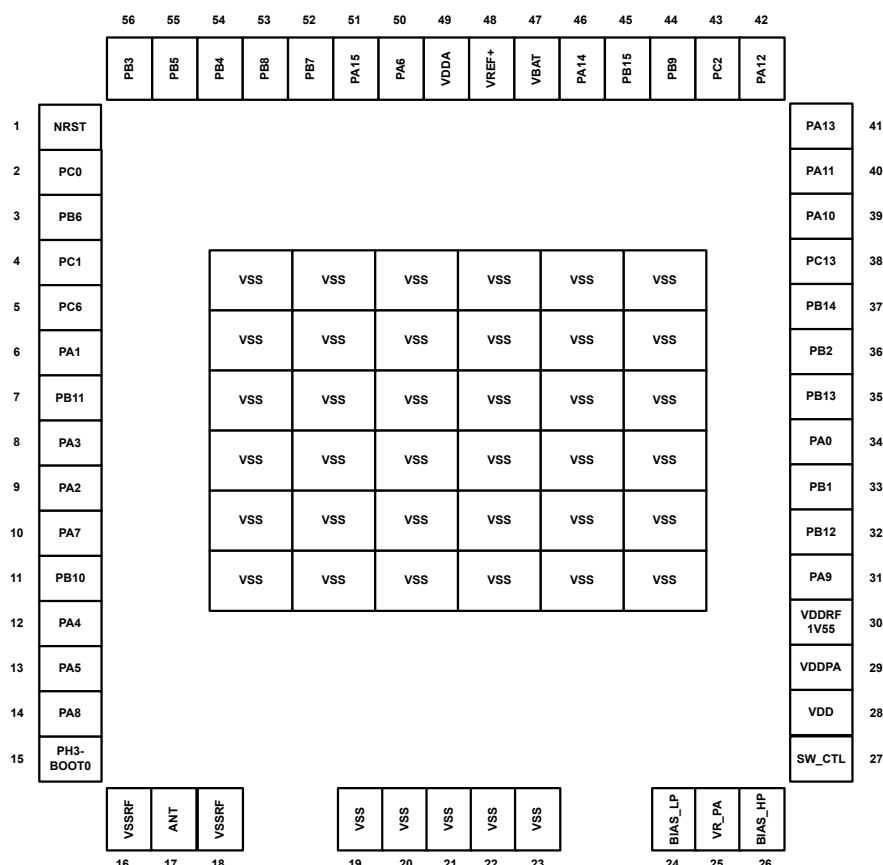
- Connecting several GPIOs to PB8 externally, and using them as supply. See the schema "STSAFE supplied by PB8 and additional GPIOs" in [Figure 10. STSAFE configurations](#).
- Adding an external switch-on VDD, controlled by a GPIO. See the schema "STSAFE supplied by on-board VDD, switchable" in [Figure 10. STSAFE configurations](#).
- Connecting VDD to PB8, and configuring PB8 in Output forced to '1'. See the schema "STSAFE supplied by on-board VDD" in [Figure 10. STSAFE configurations](#).

Figure 10. STSAFE configurations


4 Pinouts/ballouts, pin description, and alternate functions

4.1 Pinout/ballout schematics

Figure 11. SIP LGA92 pinout



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1. Package top view.

4.2 Pin description

Table 2. Legend/abbreviations used in the pinout table

| Name | Abbreviation | Definition |
|---------------|---|------------------|
| Pin name | Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name | |
| Pin type | S | Supply pin |
| | I | Input only pin |
| | I/O | Input/output pin |
| | O | Output only pin |
| I/O structure | FT | 5 V-tolerant I/O |
| | RF | Radio RF pin |
| | Option for FT I/Os | |

| Name | | Abbreviation | Definition |
|---------------|----------------------|---|---|
| I/O structure | | _f | I/O, Fm+ capable |
| | | _a | I/O, with analog switch function supplied by V _{DDA} |
| Notes | | Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset. | |
| Pin functions | Alternate functions | Functions selected through GPIOx_AFR registers | |
| | Additional functions | Functions directly selected/enabled through peripheral registers | |

Table 3. STM32WL5MOC pin definition

| Pin number | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|------------|------------------------------------|----------|---------------|-------|---|----------------------|
| SIPLGA92 | | | | | | |
| 1 | NRST | I/O | FT | - | - | - |
| 2 | PC0 | I/O | FT_f | - | LPTIM1_IN1, I2C3_SCL, LPUART1_RX, LPTIM2_IN1, CM4_EVENTOUT | - |
| 3 | PB6 | I/O | FT_f | - | LPTIM1_ETR, I2C1_SCL, USART1_TX, TIM16_CH1N, CM4_EVENTOUT | - |
| 4 | PC1 | I/O | FT_f | - | LPTIM1_OUT, SPI2_MOSI/I2S2_SD, I2C3_SDA, LPUART1_TX, CM4_EVENTOUT | - |
| 5 | PC6 | I/O | FT | - | I2S2_MCK, CM4_EVENTOUT | - |
| 6 | PA1 | I/O | FT_a | - | TIM2_CH2, LPTIM3_OUT, I2C1_SMBA, SPI1_SCK, USART2_RTS, LPUART1_RTS, DEBUG_PWR_REGLP2S, CM4_EVENTOUT | - |
| 7 | PB11 | I/O | FT_f | - | TIM2_CH4, I2C3_SDA, LPUART1_TX, COMP2_OUT, CM4_EVENTOUT | - |
| 8 | PA3 | I/O | FT_a | - | TIM2_CH4, I2S2_MCK, USART2_RX, LPUART1_RX, CM4_EVENTOUT | - |
| 9 | PA2 | I/O | FT_a | - | LSCO, TIM2_CH3, USART2_TX, LPUART1_TX, COMP2_OUT, DEBUG_PWR_LDORDY, CM4_EVENTOUT | LSCO |
| 10 | PA7 | I/O | FT_fa | - | TIM1_CH1N, I2C3_SCL, SPI1_MOSI, COMP2_OUT, DEBUG_SUBGHZSPI_MOSIOUT, TIM17_CH1, CM4_EVENTOUT | - |
| 11 | PB10 ⁽¹⁾ | I/O | FT_f | - | TIM2_CH3, I2C3_SCL, SPI2_SCK/I2S2_CK, LPUART1_RX, COMP1_OUT, CM4_EVENTOUT | - |
| 12 | PA4 | I/O | FT | - | RTC_OUT2, LPTIM1_OUT, SPI1_NSS, USART2_CK, DEBUG_SUBGHZSPI_NSSOUT, LPTIM2_OUT, CM4_EVENTOUT | - |
| 13 | PA5 | I/O | FT | - | TIM2_CH1, TIM2_ETR, SPI2_MISO, SPI1_SCK, DEBUG_SUBGHZSPI_SCKOUT, LPTIM2_ETR, CM4_EVENTOUT | - |
| 14 | PA8 | I-O | FT_a | - | MCO, TIM1_CH1, SPI2_SCK/I2S2_CK, USART1_CK, LPTIM2_OUT, CM4_EVENTOUT | - |
| 15 | PH3-BOOT0 | I/O | FT | - | CM4_EVENTOUT | BOOT0 |
| 16 | VSSRF | S | - | - | - | - |
| 17 | ANT | I/O | RF | - | - | - |
| 18 | VSSRF | S | - | - | - | - |
| 19 | VSS | S | - | - | - | - |
| 20 | VSS | S | - | - | - | - |
| 21 | VSS | S | - | - | - | - |

| Pin number | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|------------|------------------------------------|----------|---------------|-------|---|--|
| SIPLGA92 | | | | | | |
| 22 | VSS | S | - | - | - | - |
| 23 | VSS | S | - | - | - | - |
| 24 | BIAS_LP | O | RF | - | - | - |
| 25 | VR_PA | S | RF | - | - | - |
| 26 | BIAS_HP | O | RF | - | - | - |
| 27 | SW_CTL | I/O | FT | - | CM4_EVENTOUT | - |
| 28 | VDD | S | - | - | - | - |
| 29 | VDDPA | S | RF | - | - | - |
| 30 | VDDRF1V55 | S | RF | - | - | - |
| 31 | PA9 | I/O | FT_fa | - | TIM1_CH2, SPI2_NSS/I2S2_WS, I2C1_SCL, SPI2_SCK/I2S2_CK, USART1_TX, CM4_EVENTOUT | - |
| 32 | PB12 | I/O | FT | - | TIM1_BKIN, I2C3_SMBA, SPI2_NSS/I2S2_WS, LPUART1_RTS, CM4_EVENTOUT | - |
| 33 | PB1 | I/O | FT_a | - | LPUART1_RTS_DE, LPTIM2_IN1, CM4_EVENTOUT | COMP2_INP, ADC_IN5 |
| 34 | PA0 | I/O | FT_a | - | TIM2_CH1, I2C3_SMBA, I2S_CKIN, USART2_CTS, COMP1_OUT, DEBUG_PWR_REGLP1S, TIM2_ETR, CM4_EVENTOUT | PVD_IN, TAMP_IN2/ WKUP1 |
| 35 | PB13 | I/O | FT_fa | - | TIM1_CH1N, I2C3_SCL, SPI2_SCK/I2S2_CK, LPUART1_CTS, CM4_EVENTOUT | ADC_IN0 |
| 36 | PB2 | I/O | FT_a | - | LPTIM1_OUT, I2C3_SMBA, SPI1_NSS, DEBUG_RF_SMPSRDY, CM4_EVENTOUT | COMP1_INP, COMP2_INM, ADC_IN4 |
| 37 | PB14 | I/O | FT_fa | - | IM1_CH2N, I2S2_MCK, I2C3_SDA, SPI2_MISO, CM4_EVENTOUT | ADC_IN1 |
| 38 | PC13 | I/O | FT | - | CM4_EVENTOUT | TAMP_IN1/ RTC_OUT1/ RTC_TS/WKUP2 |
| 39 | PA10 | I/O | FT_fa | - | RTC_REFIN, TIM1_CH3, I2C1_SDA, SPI2_MOSI/ I2S2_SD, USART1_RX, DEBUG_RF_HSE32RDY, TIM17_BKIN, CM4_EVENTOUT | COMP1_INM, COMP2_INM, DAC_OUT1, ADC_IN6 |
| 40 | PA11 ⁽²⁾ | I/O | FT_fa | - | TIM1_CH4, TIM1_BKIN2, LPTIM3_ETR, I2C2_SDA, SPI1_MISO, USART1_CTS, DEBUG_RF_NRESET, CM4_EVENTOUT | COMP1_INM, COMP2_INM, ADC_IN7 |
| 41 | PA13 | I/O | FT_a | - | JTMS-SWDIO, I2C2_SMBA, IR_OUT, CM4_EVENTOUT | ADC_IN9 |
| 42 | PE12 ⁽³⁾ | I/O | FT_fa | - | TIM1_ETR, LPTIM3_IN1, I2C2_SCL, SPI1_MOSI, RF_BUSY, USART1_RTS, CM4_EVENTOUT | ADC_IN8 |
| 43 | PC2 | I/O | FT | - | LPTIM1_IN2, SPI2_MISO, CM4_EVENTOUT | - |
| 44 | PB9 | I/O | FT_f | - | TIM1_CH3N, I2C1_SDA, SPI2_NSS/I2S2_WS, IR_OUT, TIM17_CH1, CM4_EVENTOUT | - |
| 45 | PB15 | I/O | FT_f | - | TIM1_CH3N, I2C2_SCL, SPI2_MOSI/I2S2_SD, CM4_EVENTOUT | - |
| 46 | PA14 | I/O | FT_a | - | JTCK-SWCLK, LPTIM1_OUT, I2C1_SMBA, CM4_EVENTOUT | ADC_IN10 |
| 47 | VBAT | S | - | - | - | - |

| Pin number | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|------------|---------------------------------------|----------|---------------|-------|---|--|
| SIPLGA92 | | | | | | |
| 48 | VREF+ | S | - | - | - | - |
| 49 | VDDA | S | - | - | - | - |
| 50 | PA6 | I/O | FT | - | TIM1_BKIN, I2C2_SMBA, SPI1_MISO, LPUART1_CTS, DEBUG_SUBGHZSPI_MISOOUT, TIM16_CH1, CM4_EVENTOUT | - |
| 51 | PA15 | I/O | FT_fa | - | JTDI, TIM2_CH1, TIM2_ETR, I2C2_SDA, SPI1_NSS, CM4_EVENTOUT | COMP1_INM, COMP2_INP, ADC_IN11 |
| 52 | PB7 | I/O | FT_f | - | LPTIM1_IN2, TIM1_BKIN, I2C1_SDA, USART1_RX, TIM17_CH1N, CM4_EVENTOUT | - |
| 53 | PB8 ⁽⁴⁾ | I/O | FT_f | - | TIM1_CH2N, I2C1_SCL, RF_IRQ2, TIM16_CH1, CM4_EVENTOUT | - |
| 54 | PB4 | I/O | FT_fa | - | NJTRST, I2C3_SDA, SPI1_MISO, USART1_CTS, DEBUG_RF_LDORDY, TIM17_BKIN, CM4_EVENTOUT | COMP1_INP, COMP2_INP, ADC_IN3 |
| 55 | PB5 | I/O | FT_a | - | LPTIM1_IN1, I2C1_SMBA, SPI1_MOSI, RF_IRQ1, USART1_CK, COMP2_OUT, TIM16_BKIN, CM4_EVENTOUT | - |
| 56 | PB3 | I/O | FT_a | - | JTDO/TRACESWO, TIM2_CH2, SPI1_SCK, RF_IRQ0, USART1_RTS, DEBUG_RF_DTB1, CM4_EVENTOUT | COMP1_INM, COMP2_INM, ADC_IN2, TAMP_IN3/WKUP3 |
| 57 | VSS | S | - | - | - | - |
| 58 | VSS | S | - | - | - | - |
| 59 | VSS | S | - | - | - | - |
| 60 | VSS | S | - | - | - | - |
| 61 | VSS | S | - | - | - | - |
| 62 | VSS | S | - | - | - | - |
| 63 | VSS | S | - | - | - | - |
| 64 | VSS | S | - | - | - | - |
| 65 | VSS | S | - | - | - | - |
| 66 | VSS | S | - | - | - | - |
| 67 | VSS | S | - | - | - | - |
| 68 | VSS | S | - | - | - | - |
| 69 | VSS | S | - | - | - | - |
| 70 | VSS | S | - | - | - | - |
| 71 | VSS | S | - | - | - | - |
| 72 | VSS | S | - | - | - | - |
| 73 | VSS | S | - | - | - | - |
| 74 | VSS | S | - | - | - | - |
| 75 | VSS | S | - | - | - | - |
| 76 | VSS | S | - | - | - | - |
| 77 | VSS | S | - | - | - | - |
| 78 | VSS | S | - | - | - | - |

| Pin number | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|------------|---------------------------------------|----------|---------------|-------|---------------------|-------------------------|
| SIPLGA92 | | | | | | |
| 79 | VSS | S | - | - | - | - |
| 80 | VSS | S | - | - | - | - |
| 81 | VSS | S | - | - | - | - |
| 82 | VSS | S | - | - | - | - |
| 83 | VSS | S | - | - | - | - |
| 84 | VSS | S | - | - | - | - |
| 85 | VSS | S | - | - | - | - |
| 86 | VSS | S | - | - | - | - |
| 87 | VSS | S | - | - | - | - |
| 88 | VSS | S | - | - | - | - |
| 89 | VSS | S | - | - | - | - |
| 90 | VSS | S | - | - | - | - |
| 91 | VSS | S | - | - | - | - |
| 92 | VSS | S | - | - | - | - |

- For STM32WL5MOCH6S, this GPIO controls the STSAFE reset, which can be controlled by your own FW
- It must be used only as I2C2_SCL on STM32WL5MOCH6S.
- It must be used only as I2C2_SCL on STM32WL5MOCH6S.
- It must be used only as STSAFE supply on STM32WL5MOCH6S.

4.3 Alternate functions

Table 4. Alternate function AF0 to AF7

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|--------|------|-----------|----------------------|------------|----------------------|--------------------|-----------------------|---------|-------------------|
| | | SYS_AF | TIM1/TIM2/ LPTIM1 | TIM1/TM2 | SPI2/ TIM1/LPTIM3 | I2C1/I2C2/ I2C3 | SPI1/SPI2S2 | RF | USART1/ USART2 |
| Port A | PA0 | - | TIM2_CH1 | - | - | I2C3_SMBA | I2S_CKIN | - | USART2_CTS |
| | PA1 | - | TIM2_CH2 | - | LPTIM3_OUT | I2C1_SMBA | SPI1_SCK | - | USART2_RTS |
| | PA2 | LSCO | TIM2_CH3 | - | - | - | - | - | USART2_TX |
| | PA3 | - | TIM2_CH4 | - | - | - | I2S2_MCK | - | USART2_RX |
| | PA4 | RTC_OUT2 | LPTIM1_OUT | - | - | - | SPI1_NSS | - | USART2_CX |
| | PA5 | - | TIM2_CH1 | TIM2_ETR | SPI2_MISO | - | SPI1_SCK | - | - |
| | PA6 | - | TIM1_BKIN | - | - | I2C2_SMBA | SPI1_MISO | - | - |
| | PA7 | - | TIM1_CH1N | - | - | I2C3_SCL | SPI1_MOSI | - | - |
| | PA8 | MCO | TIM1_CH1 | - | - | - | SPI2_SCK/ I2S2_CK | - | USART1_CK |
| | PA9 | - | TIM1_CH2 | - | SPI2_NSS/ I2S2_WS | I2C1_SCL | SPI2_SCK/ I2S2_CK | - | USART1_TX |
| | PA10 | RTC_REFIN | TIM1_CH3 | - | - | I2C1_SDA | SPI2_MOSI/ I2S2_SD | - | USART1_RX |
| | PA11 | - | TIM1_CH4 | TIM1_BKIN2 | LPTIM3_ETR | I2C2_SDA | SPI1_MISO | - | USART1_CTS |
| | PA12 | - | TIM1_ETR | - | LPTIM3_IN1 | I2C2_SCL | SPI1_MOSI | RF_BUSY | USART1_RTS |

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|--------|------|-------------------|----------------------|----------|-----------------------|--------------------|-----------------------|---------|-------------------|
| | | SYS_AF | TIM1/TIM2/ LPTIM1 | TIM1/TM2 | SPI2/ TIM1/LPTIM3 | I2C1/I2C2/ I2C3 | SPI1/SPI2S2 | RF | USART1/ USART2 |
| Port A | PA13 | JTMS/ SWDIO | - | - | - | I2C2_SMBA | - | - | - |
| | PA14 | JTCK/ SWCLK | LPTIM1_OUT | - | - | I2C1_SMBA | - | - | - |
| | PA15 | JTDI | TIM2_CH1 | TIM2_ETR | - | I2C1_SDA | SPI1_NSS | - | - |
| Port B | PB1 | - | - | - | - | - | - | - | - |
| | PB2 | - | LPTIM1_OUT | - | - | I2C3_SMBA | SPI1_NSS | - | - |
| | PB3 | JTDO/ TRACESWO | TIM2_CH2 | - | - | - | SPI1_SCK | RF_IRQ0 | USART1_RTS |
| | PB4 | NJTRST | - | - | - | I2C3_SDA | SPI1_MISO | - | USART1_CTS |
| | PB5 | - | LPTIM1_IN1 | - | - | I2C1_SMBA | SPI1_MOSI | RF_IRQ1 | USART1_CK |
| | PB6 | - | LPTIM1_ETR | - | - | I2C1_SCL | - | - | USART1_TX |
| | PB7 | - | LPTIM1_IN2 | - | TIM1_BKIN | I2C1_SDA | - | - | USART1_RX |
| | PB8 | - | TIM1_CH2N | - | - | I2C1_SCL | - | RF_IRQ2 | - |
| | PB9 | - | TIM1_CH3N | - | - | I2C1_SDA | SPI2_NSS/ I2S2_WS | - | - |
| | PB10 | - | TIM2_CH3 | - | - | I2C3_SCL | SPI2_SCK/ I2S2_CK | - | - |
| | PB11 | - | TIM2_CH4 | - | - | I2C3_SDA | - | - | - |
| | PB12 | - | TIM1_BKIN | - | TIM1_BKIN | I2C3_SMBA | SPI2_NSS/ I2S2_WS | - | - |
| | PB13 | - | TIM1_CH1N | - | - | I2C3_SCL | SPI2_SCK/ I2S2_CK | - | - |
| | PB14 | - | TIM1_CH2N | - | I2S2_MCK | I2C3_SDA | SPI2_MISO | - | - |
| | PB15 | - | TIM1_CH3N | - | - | I2C2_SCL | SPI2_MOSI/ I2S2_SD | - | - |
| Port C | PC0 | - | LPTIM1_IN1 | - | - | I2C3_SCL | - | - | - |
| | PC1 | - | LPTIM1_OUT | - | SPI2_MOSI/ I2S2_SD | I2C3_SDA | - | - | - |
| | PC2 | - | LPTIM1_IN2 | - | - | - | SPI2_MISO | - | - |
| | PC6 | - | - | - | - | - | I2S2_MCK | - | - |
| | PC13 | - | - | - | - | - | - | - | - |
| Port H | PH3 | - | - | - | - | - | - | - | - |

Table 5. Alternate function AF8 to AF15

See Table 4 for AF0 to AF7.

| Port | | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|--------|------|--------------------|-----|------|------|----------------------|-----------------------------|-----------------------------|--------------|
| | | LPUART1 | - | - | - | COMP1/ COMP2/TIM1 | DEBUG | TIM2/TIM16/ TIM17/LPTIM2 | EVENOUT |
| Port A | PA0 | - | - | - | - | COMP1_OUT | DEBUG_PWR_RE GLP1S | TIM2_ETR | CM4_EVENTOUT |
| | PA1 | LPUART1_RTS | - | - | - | - | DEBUG_PWR_RE GLP2S | - | |
| | PA2 | LPUART1_TX | - | - | - | COMP2_OUT | DEBUG_PWR_LD ORDY | - | |
| | PA3 | LPUART1_RX | - | - | - | - | - | - | |
| | PA4 | - | - | - | - | - | DEBUG_SUBGHZ SPI_NSSOUT | LPTIM2_OUT | |
| | PA5 | - | - | - | - | - | DEBUG_SUBGHZ SPI_SCKOUT | LPTIM2_ETR | |
| | PA6 | LPUART1_CTS | - | - | - | TIM1_BKIN | DEBUG_SUBGHZ SPI_MISOOUT | TIM16_CH1 | |
| | PA7 | - | - | - | - | COMP2_OUT | DEBUG_SUBGHZ SPI_MOSIOUT | TIM17_CH1 | |
| | PA8 | - | - | - | - | - | - | LPTIM2_OUT | |
| | PA9 | - | - | - | - | - | - | - | |
| | PA10 | - | - | - | - | - | DEBUG_RF_HSE3 2RDY | TIM17_BKIN | |
| | PA11 | - | - | - | - | TIM1_BKIN2 | DEBUG_RF_NRE SET | - | |
| | PA12 | - | - | - | - | - | - | - | |
| | PA13 | IR_OUT | - | - | - | - | - | - | |
| | PA14 | - | - | - | - | - | - | - | |
| | PA15 | - | - | - | - | - | - | - | |
| Port B | PB1 | LPUART1_ RTS_DE | - | - | - | - | - | LPTIM2_IN1 | |
| | PB2 | - | - | - | - | - | DEBUG_RF_SMP SRDY | - | |
| | PB3 | - | - | - | - | - | DEBUG_RF_DTB1 | - | |
| | PB4 | - | - | - | - | - | DEBUG_RF_LDO RDY | TIM17_BKIN | |
| | PB5 | - | - | - | - | COMP2_OUT | - | TIM16_BKIN | |
| | PB6 | - | - | - | - | - | - | TIM16_CH1N | |
| | PB7 | - | - | - | - | - | - | TIM17_CH1N | |
| | PB8 | - | - | - | - | - | - | TIM16_CH1 | |
| | PB9 | IR_OUT | - | - | - | - | - | TIM17_CH1 | |
| | PB10 | LPUART1_RX | - | - | - | COMP1_OUT | - | - | |
| | PB11 | LPUART1_TX | - | - | - | COMP2_OUT | - | - | |
| | PB12 | LPUART1_RTS | - | - | - | - | - | - | |
| | PB13 | LPUART1_CTS | - | - | - | - | - | - | |
| | PB14 | - | - | - | - | - | - | - | |
| | PB15 | - | - | - | - | - | - | - | |

| Port | | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|--------|------|------------|-----|------|------|----------------------|-------|-----------------------------|--------------|
| | | LPUART1 | - | - | - | COMP1/ COMP2/TIM1 | DEBUG | TIM2/TIM16/ TIM17/LPTIM2 | EVENOUT |
| Port C | PC0 | LPUART1_RX | - | - | - | - | - | LPTIM2_IN1 | CM4_EVENTOUT |
| | PC1 | LPUART1_TX | - | - | - | - | - | - | |
| | PC2 | - | - | - | - | - | - | - | |
| | PC6 | - | - | - | - | - | - | - | |
| | PC13 | - | - | - | - | - | - | - | |
| Port H | PH3 | - | - | - | - | - | - | - | |

5 Electrical characteristics

5.1 Operating conditions

Table 6. STM32WL5MOC operating conditions

| Parameter | Min. | Typ. | Max. | Unit |
|-------------------------------------|------|------|------|------|
| V _{DD} | 1.71 | 3.3 | 3.6 | V |
| Operating ambient temperature range | -40 | - | 85 | °C |
| Storage temperature range | -40 | - | 125 | °C |

5.2 Power consumption

Refer to Multiprotocol LPWAN dual core 32-bit Arm® Cortex®- M4/M0+ LoRa® (G)FSK, (G)MSK, BPSK (DS13293) for more details.

The power consumption is identical to the STM32WL55xx. Refer to Multiprotocol LPWAN dual core 32-bit Arm® Cortex®- M4/M0+ LoRa® (G)FSK, (G)MSK, BPSK (DS13293) for all power consumption figures, except for tables *Sub-GHz radio power consumption* and *Sub-GHz radio power consumption in transmit mode*, that you can find below. This power consumption modification takes into account the presence of a 32MHz TCXO inside the module.

Table 7. Sub-GHz radio power consumption

| Symbol | Mode | Conditions | Min | Typ | Max | Unit |
|-----------------|---|--|----------------------------|------|-------|------|
| I _{DD} | Deep-Sleep mode (Sleep with cold start) | All blocks off | - | 50 | - | nA |
| | Sleep mode (with warm start) | Configuration retained | - | 140 | - | |
| | | Configuration retained + RC64k | - | 810 | - | |
| | Sleep, LDO mode | LDO, band-gap, RC 13 MHz on | - | 414 | - | μA |
| | | HSE32 off | | 564 | - | |
| | Sleep, SMPS mode | Band-gap, RC 13 MHz on, SMPS 40 mA max | - | 700 | - | |
| | | HSE32 on | | 950 | - | |
| | Standby mode (RC 13 MHz on) | RC 13 MHz on, HSE32 off | - | 0.7 | - | mA |
| | Standby mode (HSE32) | SMPS mode | - | 2.55 | - | |
| | | 40 mA max settings | | 2.49 | - | |
| | Synthesizer mode | LDO mode | - | 4.16 | - | |
| | | SMPS mode used with 40 mA drive capability | - | 5.55 | - | |
| | Receive mode, SMPS mode used | SMPS 40 mA max | FSK 4.8 Kbit/s | - | 5.97 | mA |
| | | | LoRa 125 kHz | - | 6.32 | |
| | | | Rx boosted, FSK 4.8 Kbit/s | - | 6.62 | |
| | | | RX boosted, LoRa 125 kHz | - | 6.96 | |
| | Receive mode, LDO mode used | Rx boosted | FSK 4.8 Kbit/s | - | 9.68 | |
| | | | LoRa 125 kHz | - | 10.4 | |
| | | | FSK 4.8 Kbit/s | - | 11.02 | |
| | | | LoRa 125 kHz | - | 11.72 | |

1. Cold start is equivalent to device at POR or when the device wakes up from Sleep mode with all blocks off.
2. Only Sub-GHz radio power consumption
3. Warm start only happens when the device wakes up from Sleep mode with its configuration retained
4. System in Stop 0 mode range 2

Table 8. Sub-GHz radio power consumption and effective transmitted output power in [868 to 915]MHz band

| Symbol | Frequency band (MHz) | PA match (conditions) | Programmed power output | Measured power output | | | |
|--------|----------------------|-----------------------|------------------------------------|-----------------------|------|------|------|
| | | | | Typ (LDD) | Unit | Typ | Unit |
| < | 868 to 915 | Low power | +10 dBm, $V_{DDRF} = 3.3\text{ V}$ | 20 | mA | 9.2 | dBm |
| | | | +10 dBm, $V_{DDRF} = 1.8\text{ V}$ | 35 | | 9.1 | |
| | | | +15 dBm, $V_{DDRF} = 3.3\text{ V}$ | 29 | | 13.7 | |
| | | | +15 dBm, $V_{DDRF} = 1.8\text{ V}$ | 52 | | 13.4 | |
| | | High power | +22 dBm, $V_{DDRF} = 3.3\text{ V}$ | 111 | | 20.3 | |
| | | | +22 dBm, $V_{DDRF} = 1.8\text{ V}$ | 80 | | 16 | |
| | | | +20 dBm, $V_{DDRF} = 3.3\text{ V}$ | 103 | | 18.6 | |
| | | | +20 dBm, $V_{DDRF} = 1.8\text{ V}$ | 80 | | 16 | |

1. These power outputs correspond to the settings programmed in the device. Depending on the board, up to 2 dB less than the setting are expected.

5.3 32 MHz TCXO clock characteristics

The embedded 32 MHz TCXO clock has the following characteristics:

Table 9. STM32WL5M TCXO characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--------|--------------------|----------------------------|------|------|------|------|
| Fnom | Output frequency | | - | 32 | - | MHz |
| Ftol | Frequency accuracy | Initial | -2.0 | - | +2.0 | ppm |
| | | Over temperature [-40:+85] | -1.0 | - | +1.0 | |
| | | Aging over 10 years | -10 | - | +10 | |

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 Device marking

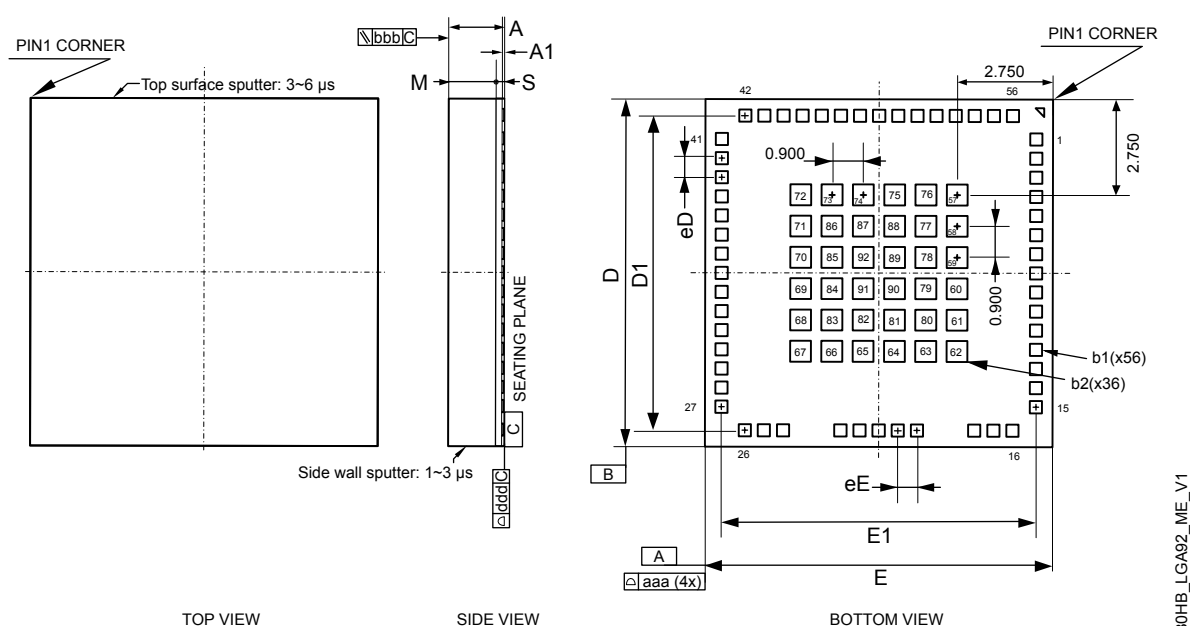
Refer to the technical note "Reference device marking schematics for STM32 microcontrollers and microprocessors" (TN1433) available on www.st.com, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

Parts marked as "ES", "E" or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

6.2 LGA92 package information

This LGA is a 92 lead, 10 x 10 mm, 1.608 mm pitch, lead grid array package.

Figure 12. LGA92 - Outline



1. Drawing is not to scale.

Table 10. LGA92 - Mechanical data

| Symbol | millimeters | | | inches ⁽¹⁾ | | |
|-------------------|-------------|--------|--------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | 1.818±0.060 | | | 0.0716±0.0024 | | |
| A1 | 0.030±0.020 | | | 0.0012±0.0008 | | |
| b1 ⁽²⁾ | 0.350x0.350 | | | 0.0138x0.0138 | | |
| b2 ⁽³⁾ | 0.600x0.600 | | | 0.0236x0.0236 | | |
| D | 9.900 | 10.000 | 10.100 | 0.3898 | 0.3937 | 0.3976 |
| D1 | 9.050 | | | 0.3563 | | |
| eD | 0.550 | | | 0.0216 | | |
| E | 9.900 | 10.000 | 10.100 | 0.3898 | 0.3937 | 0.3976 |
| E1 | 9.050 | | | 0.3563 | | |
| eE | 0.550 | | | 0.0216 | | |
| M | 1.540 | | | 0.0606 | | |
| S | 0.248 | | | 0.0098 | | |
| n | 92 | | | | | |
| aaa | 0.100 | | | 0.0039 | | |
| bbb | 0.100 | | | 0.0039 | | |
| ddd | 0.100 | | | 0.0039 | | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Peripheral pad.
3. Inner pad.

6.3 Thermal characteristics

The thermal characteristics of the STM32WL5MOC are defined below and the constant values are given in Table 11 where:

- Θ_{JA} , is the junction-to-ambient thermal resistance (EIA/JESD51-2 and EIA/JESD51-6).
 Θ_{JA} represents the resistance to the heat flows from the chip to ambient air. It is an indicator of package heat dissipation capability. Lower Θ_{JA} , means better overall thermal performance and is calculated as follows:

$$\Theta_{JA} = (T_J - T_A) / P_H$$
 where:
 - T_J = junction temperature
 - T_A = ambient temperature
 - P_H = power dissipation.
- Ψ_{JT} is the junction-to-top-center thermal characterization parameter (EIA/JESD51-2 and EIA/JESD51-6).
 Ψ_{JT} is used for estimating the junction temperature by measuring T_T in an actual environment and is calculated as follows:

$$\Psi_{JT} = (T_J - T_T) / P_H$$
 where T_T = temperature at the top-center of the package.
- Θ_{JC} is the junction-to-case thermal resistance.
 Θ_{JC} represents the resistance to the heat flows from the chip to package top case. Θ_{JC} is important when external heat sink is attached on package top and is calculated as follows:

$$\Theta_{JC} = (T_J - T_C) / P_H$$
 where T_C = case temperature attached with a cold plate.
- Θ_{JB} is the junction-to-board thermal resistance (EIA/JESD51-8).
 Θ_{JB} represents the resistance to the heat flows from the chip to PCB. Θ_{JB} is used in compact thermal models for system-level thermal simulation and is calculated as follows:

$$\Theta_{JB} = (T_J - T_B) / P_H$$
 where T_B = board temperature with ring cold plate fixture applied.

Table 11. STM32WL5MOC thermal characteristics

| Symbol | $T_J(^{\circ}\text{C})$ | $T_T(^{\circ}\text{C})$ | $\Psi_{JT}(^{\circ}\text{C/W})$ | $\Theta_{JA}(^{\circ}\text{C/W})$ | $\Theta_{JB}(^{\circ}\text{C/W})$ | $\Theta_{JC}(^{\circ}\text{C/W})$ |
|--------|-------------------------|-------------------------|---------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|
| Value | 96.79 | 96.70 | 0.20 | 25.96 | 11.49 | 9.59 |

7 Ordering information

Table 12. Ordering information

| Order code | STSAFE-A110 | Flash size | Temperature range | Package type | Pin count | Packing information |
|------------------|--------------------------------|------------|--|--------------|-----------|---------------------|
| STM32WL5MOCH6STR | STSAFE-A110 is provisioned | 256 Kbytes | Industrial temperature range, -40 to 85 °C (105 °C junction) | LGA | 92 | Tape and reel |
| STM32WL5MOCH6TR | STSAFE-A110 is not provisioned | 256 Kbytes | Industrial temperature range, -40 to 85 °C (105 °C junction) | LGA | 92 | Tape and reel |

Note: For a list of available options (such as speed and package) or for further information on any aspect of this device, contact your nearest ST sales office.

8 FCC - ISED compliance statement

FCC Part 15 compliance statement

Changes or modifications not expressly approved by STMicroelectronics could void the user's authority to operate the equipment.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

- This module has been approved under FCC part 15C 15.247. This modular transmitter is only FCC authorized for this specific rule part.
- The module is limited to OEM installation ONLY.
- The OEM integrator is responsible for ensuring that the end-user has no manual instruction to remove or install the module.
- The host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. (For example, Part 15 Subpart B)
- If testing of the host product with this transmitter installed and operating is necessary (to verify that the host product meets all the applicable FCC rules), a test mode for this specific module is available upon request to STMicroelectronics.
- Trace antenna design, and professional installation is not applicable to this modular certification.
- List of antenna types approved: Dipole antenna with max gain 2 dBi.

Radio Frequency (RF) Exposure Compliance of Radio communication

- High output power: To satisfy FCC RF Exposure requirements, a separation distance of 20 cm or more should be maintained between the antenna of this device and persons during operation. To ensure compliance, operation at a closer distance than this is not recommended. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.
- Low output power: To satisfy FCC RF Exposure requirements, a separation distance of 27mm or more should be maintained between the antenna of this device and persons during operation. To ensure compliance, operation at a closer distance than this is not recommended. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

ISED - Industry Canada Licence-Exempt Radio Apparatus

This device contains licence-exempt transmitter(s)/receivers(s) that comply with Innovation, Science and Economic Development Canada's licence-exempt RSS(s). Operation is subject to the following two conditions:

1. This device may not cause interference.
2. This device must accept any interference, including interference that may cause undesired operation of the device.

ISED - Industrie Canada appareil radio exempts de licence

L'émetteur/récepteur exempt de licence contenu dans le présent appareil est conforme aux CNR d'innovation, Sciences et Développement économique Canada applicables aux appareils radio exempts de licence.

L'exploitation est autorisée aux deux conditions suivantes:

1. L'appareil ne doit pas produire de brouillage.
2. L'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

This module has been approved under RSS-247. This modular transmitter is only ISED-Canada authorized for this specific rule part.

- The module is limited to OEM installation ONLY.
- The OEM integrator is responsible for ensuring that the end-user has no manual instruction to remove or install module.
- The host product manufacturer is responsible for compliance to any other ISED rules that apply to the host not covered by the modular transmitter grant of certification. (For example, ICES-003).
- If testing of the host product with this transmitter installed and operating is necessary (to verify that the host product meets all the applicable ISED rules), a test mode for this specific module is available upon request to STMicroelectronics.
- Trace antenna design, and professional installation is not applicable to this modular certification.
- List of antenna types approved: Dipole antenna with max gain 2 dBi.

Radio Frequency (RF) Exposure Compliance of Radio communication for mobile Apparatus

- High output power: To satisfy ISED-Canada RF Exposure requirements, a separation distance of 20 cm or more should be maintained between the antenna of this device and persons during operation. To ensure compliance, operation at a closer distance than this is not recommended. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.
- Low output power: To satisfy ISED-Canada RF Exposure requirements, a separation distance of 35mm or more should be maintained between the antenna of this device and persons during operation. To ensure compliance, operation at a closer distance than this is not recommended. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

End Product Labeling

FCC Certification

The final end product must be labeled in a visible area with the following: *"Contains Transmitter Module FCC:YCP-32WL5MOCH01"*

ISED Certification

The final end product must be labeled in a visible area with the following:

L'équipement final doit être étiqueté sur un endroit visible avec le texte suivant :

"Contains Transmitter Module IC: 8976A-32WL5MOCH01"

End Product User's Manual:

The user manual for end users must include the following information in a prominent location:

- High output power: To satisfy FCC RF Exposure requirements, a separation distance of 20 cm or more should be maintained between the antenna of this device and persons during operation. To ensure compliance, operation at a closer distance than this is not recommended. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.
- Low output power: To satisfy FCC RF Exposure requirements, a separation distance of 27mm or more should be maintained between the antenna of this device and persons during operation. To ensure compliance, operation at a closer distance than this is not recommended. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.
- High output power: To satisfy ISED-Canada RF Exposure requirements, a separation distance of 20 cm or more should be maintained between the antenna of this device and persons during operation. To ensure compliance, operation at a closer distance than this is not recommended. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.
- Low output power: To satisfy ISED-Canada RF Exposure requirements, a separation distance of 35mm or more should be maintained between the antenna of this device and persons during operation. To ensure compliance, operation at a closer distance than this is not recommended. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Important security notice

The STMicroelectronics group of companies (ST) places a high value on product security, which is why the ST product(s) identified in this documentation may be certified by various security certification bodies and/or may implement our own security measures as set forth herein. However, no level of security certification and/or built-in security measures can guarantee that ST products are resistant to all forms of attacks. As such, it is the responsibility of each of ST's customers to determine if the level of security provided in an ST product meets the customer needs both in relation to the ST product alone, as well as when combined with other components and/or software for the customer end product or application. In particular, take note that:

- ST products may have been certified by one or more security certification bodies, such as Platform Security Architecture (www.psacertified.org) and/or Security Evaluation standard for IoT Platforms (www.trustcb.com). For details concerning whether the ST product(s) referenced herein have received security certification along with the level and current status of such certification, either visit the relevant certification standards website or go to the relevant product page on www.st.com for the most up to date information. As the status and/or level of security certification for an ST product can change from time to time, customers should re-check security certification status/level as needed. If an ST product is not shown to be certified under a particular security standard, customers should not assume it is certified.
- Certification bodies have the right to evaluate, grant and revoke security certification in relation to ST products. These certification bodies are therefore independently responsible for granting or revoking security certification for an ST product, and ST does not take any responsibility for mistakes, evaluations, assessments, testing, or other activity carried out by the certification body with respect to any ST product.
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Revision history

Table 13. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 08-Nov-2023 | 1 | Initial release. |
| 21-Dec-2023 | 2 | Updated the following sections: <ul style="list-style-type: none"> Section Device summary Section 2: Description Section 8: FCC - ISED compliance statement Section 7: Ordering information Section 3.4: RF antenna impact Section 3.5.2: STSAFE supply |
| 04-Jan-2024 | 3 | Updated the Section 7: Ordering information and the Section Cover image |

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