a module solution provider

WG3221E00

WG3221-00 Evaluation Board

User Guide

Drift 0.2

Prepared By	Reviewed By	Approved By

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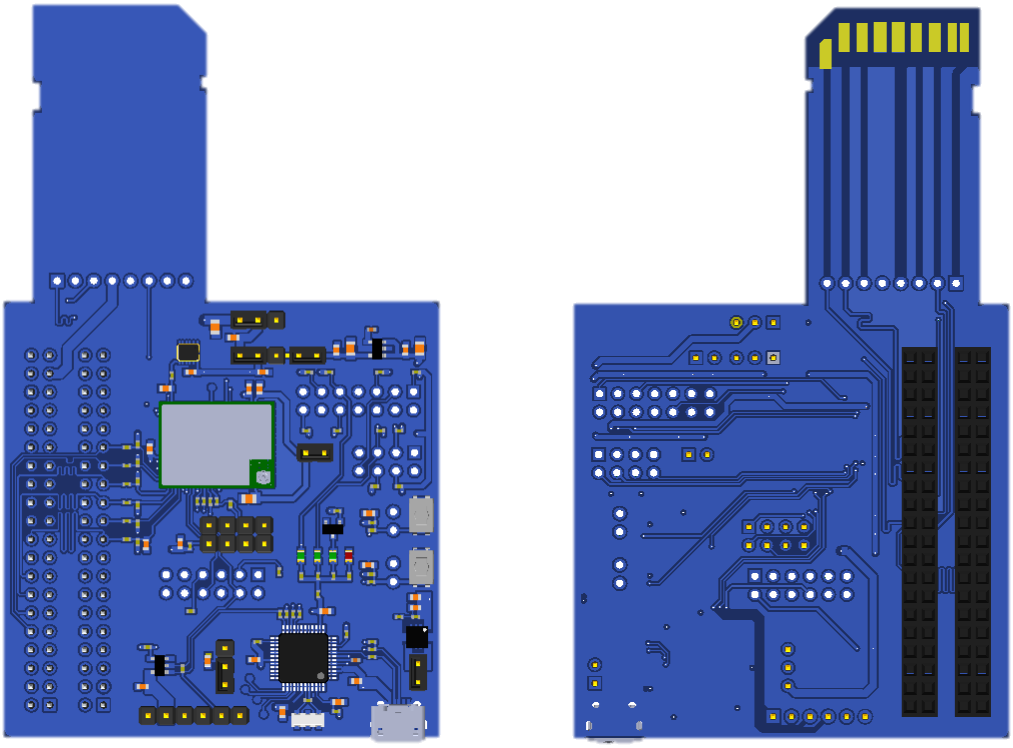
1. INTRODUCTION

The WG3221-00 is a wireless local area network (WLAN) and Bluetooth (BT) combination module to support 1 × 1 IEEE 802.11a/b/g/n/ac WLAN standards and BT5.0. This document is a user guide for the Jorjin WG3221-00 Evaluation Board. The WG3221E00 EVB is configured to SDIO for WLAN interface, as well as UART for Bluetooth.

This document is intended primarily for configuring the WG3221-00 for connectivity testing in the lab.



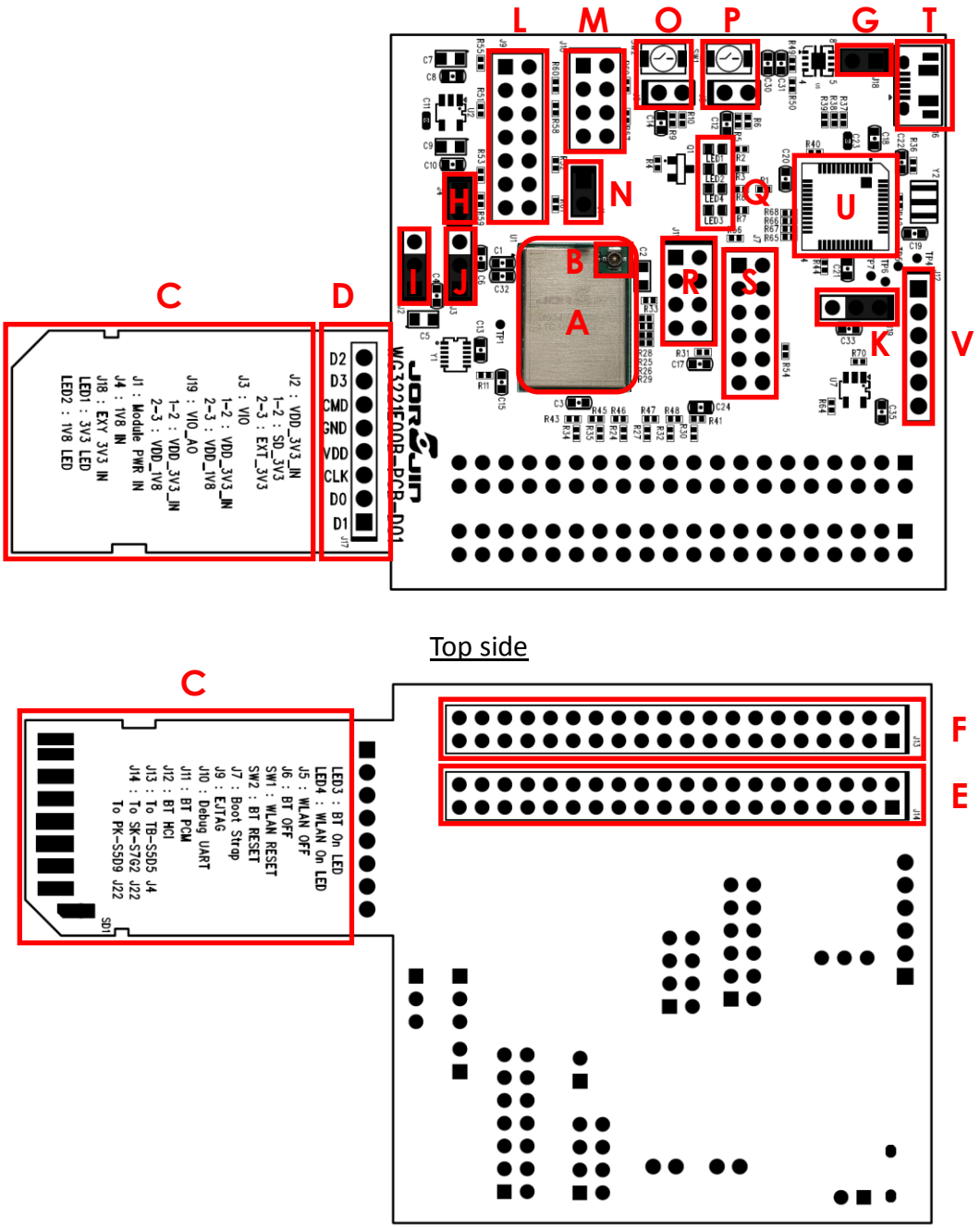
TOP side **Bottom side**

Figure 1-1. WG32210-00 Evaluation Board

2. HARDWARE DESCRIPTION

2.1. Board Overview

The following figure and table describe physical sections of the board.



Top side

Bottom side

Figure 2-1. WG3221E00 board Components

Table 2-1. WG3221E00 board component descriptions

Region	Description
A	WG3221-00 module
B	WLAN/BT RF signal I-PEX connector (part Number：20449-001E)
C	SDIO card for WLAN
D	WLAN SDIO signals for measurement
E	WLAN SDIO signals for Renesas SK-S7G2 and PK-S5D9 evaluation board CONN J22
F	WLAN SDIO signals for Renesas TB-S5D5 evaluation board CONN J4
G	Current measurement jumper for EXT 3.3V power.
H	Current measurement jumper for 1.8V power
I	3.3V power source selection
J	VIO power source selection
K	VIO_AO power source selection
L	EJTAG debug mode connector. Not used.
M	Debug UART connector. Not used.
N	Current measurement jumper for 3.3V power of WG3221-00 module
O	BT function reset switch and jumper.
P	WLAN function reset switch and jumper.
Q	LED indicators
R	BT PCM signals connector.
S	Boot Strap/DEBUG connector. Not used.
T	UART to USB connector for BT function test.
U	UART to USB chip for BT function test.
V	BT HCI UART signals for measurement or connecting to external circuit.

2.2. Power Supply

- The 3.3V power source of module select by J2 (Figure 2-1. Region I)：
  - SD_3V3：SD1 (Figure 2-1. Region C)、J13 (Figure 2-1. Region F) or J14 (Figure 2-1. Region E)
  - External_3V3 (via the 5V to 3.3V LDO)：J18 (Figure 2-1. Region G)

Table 2-2. WG3221E00 VIO power supply modes

3.3V power level	J2	Comment
SD_3V3	Fitted：1-2	The power supplied from SD1、J13、J14.
External_3V3	Fitted：2-3	The power supplied from J18.

- The 1.8V power source (via the 3.3V to 1.8V LDO)：(Figure 2-1. Region H).
- J3 sets the VIO power level. (Figure 2-1. Region J)

Table 2-3. WG3221E00 VIO power supply modes

VIO power level	J3	Comment
3.3V	Fitted：1-2	The I/O pins signal level is 3.3V
1.8V	Fitted：2-3	The I/O pins signal level is 1.8V

- J19 sets the VIO_A0 power level. (Figure 2-1. Region K)

Table 2-4. WG3221E00 VIO_A0 power supply modes

VIO_A0 power level	J19	Comment
3.3V	Fitted：1-2	The I/O pins signal level is 3.3V
1.8V	Fitted：2-3	The I/O pins signal level is 1.8V

2.3. SDIO interfaces

There are four SDIO connectors in the WG3221E00 for WLAN interface. The host CPU can be connected to SDIO interface through either one of the connectors.

Table 2-5. WG3221E00 SDIO interface

Connector	Region	Description
SD1	C	Standard SDIO card
J17	D	For external SDIO interface
J14	E	WLAN SDIO signals for Renesas SK-S7G2 and PK-S5D9 evaluation board CONN J22
J13	F	WLAN SDIO signals for Renesas TB-S5D5 evaluation board CONN J4

2.4. HCI UART interface

The host CPU can be connected to HCI interface through the J12 (Figure 2-1. Region W). When the J12 is connected to host CPU, the R65,R66,R67,R68 must be removed.

The HCI UART can be also connected through USB –J16 (Figure 2-1. Region T). When the J16 is connected to USB host, the R65,R66,R67,R68 must be installed.

2.5. PCM/I2S interface

The BT PCM signals are connected to J11 (Figure 2-1. Region R).

2.6. LEDs

There are 4 LEDs (Figure 2-1. Region Q) indicate the board status.

Table 2-5：WG3221E00 LEDs

LED #	Description
LED1	It indicates the board is being powered 3.3V.
LED2	It indicates the board is being powered 1.8V.
LED3	It indicates the BT function.
LED4	It indicates the WLAN function.

2.7. WLAN/BT reset or off

The board has two buttons to reset the WLAN and BT function (Figure 2-1. Region O and P). The board also has two jumpers to turn off the WLAN and BT function.

Table 2-6：WG3221E00 WLAN/BT reset and turn off

Button #	Jumper #	Description
SW1	J5	Push the button to reset or fit the jumper to turn off WLAN function
SW2	J6	Push the button to reset or fit the jumper to turn off BT function

3. CONNECTING TO PLATFORM

3.1. General Connection

WLAN function：SDMMC card for SDIO interface. Connect to platform SD connector.

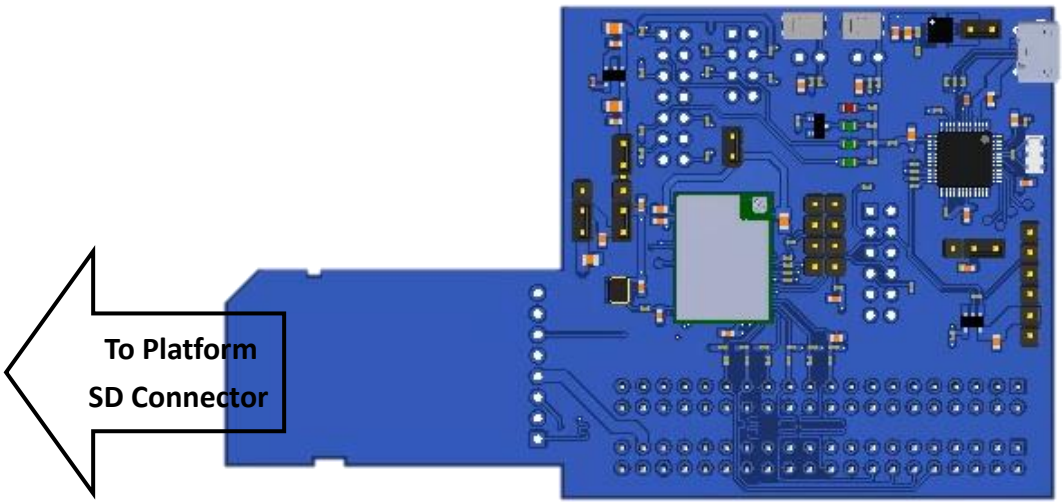


Figure 3-1：SDMMC for SDIO interface

Bluetooth function：Both Micro USB and 1X6 pin header for UART interface.
Connect to PC with USB cable or connect to platform with jump-wire.

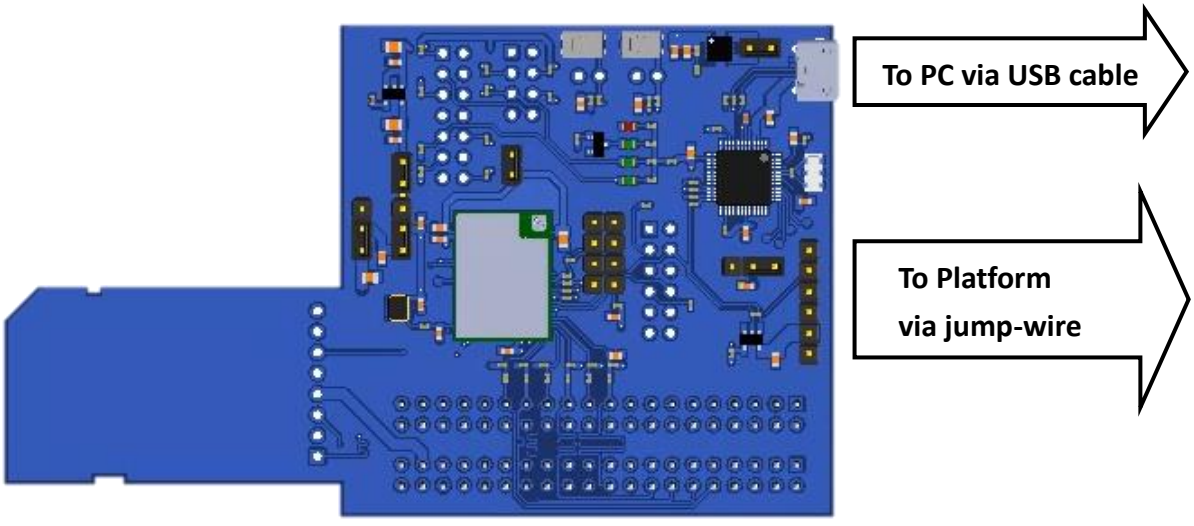
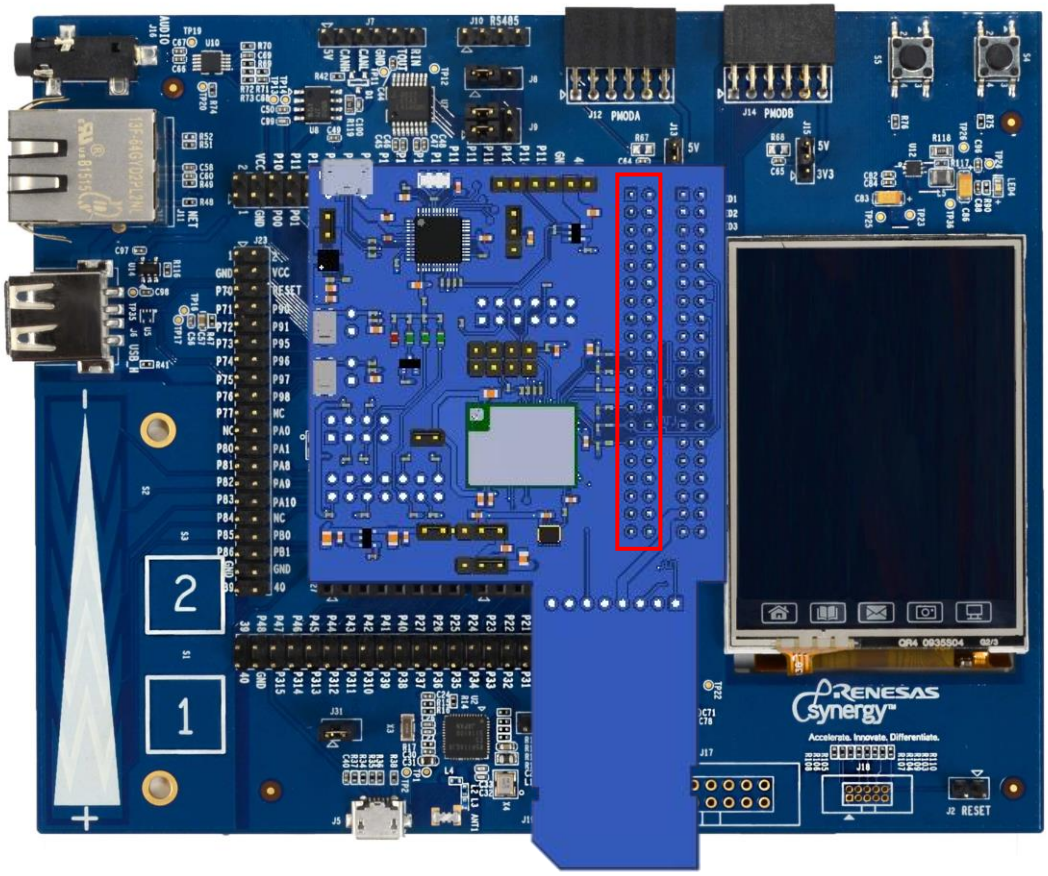


Figure 3-2：Micro USB and pin header for Bluetooth interface

3.2. Renesas SK-S7G2 and PK-S5D9 platform

WLAN function：The female header J14 connect to the Renesas SK-S7G2 and PK-S5D9 platform J22.

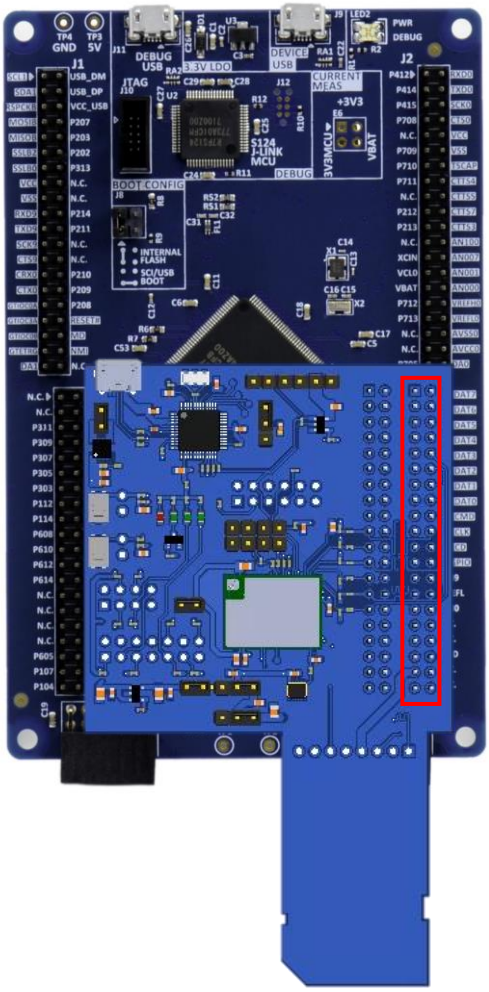


WG3221E00 J14 pin define		SK-S7G2 / PK-S5D9 J22 pin define	
3	GND	3	GND
4	VDD_MCRSD	4	VCC (+3V3)
19	SDIO_CLK	19	P5_0
21	SDIO_CMD	21	P5_1
23	SDIO_D0	23	P5_2
25	SDIO_D1	25	P5_3
27	SDIO_D2	27	P5_4
29	SDIO_D3	29	P5_5

Figure 3-3：Connect to Renesas SK-S7G2 and PK-S5D9 platform.

3.3. Renesas TB-S5D5 platform

WLAN function：The female header J13 connect to the Renesas TB-S5D5 platform J4.



WG3221E00 J13 pin define		Renesas TB-S5D5 J4 pin define	
10	SDIO_D3	10	P5_5
12	SDIO_D2	12	P5_4
14	SDIO_D1	14	P5_3
16	SDIO_D0	16	P5_2
18	SDIO_CMD	18	P5_1
20	SDIO_CLK	20	P5_0
36	GND	36	GND
37	VDD_MCRSD	37	VCC (+3V3)

Figure 3-4：SDIO interface connect to Renesas TB-S5D5 platform.

Bluetooth function：The header J12 connect to the Renesas TB-S5D5 platform J2 via jump-wire.

WG3221E00 J12 pin define		Renesas TB-S5D5 J2 pin define	
1	UART_TXD	2	P410
2	UART_RXD	4	P101
3	UART_CTS	6	P102
4	UART_RTS	8	P413
5	VDD_MCRSD	10	VCC (+3V3)
6	GND	12	GND

4. SCHEMATIC DIAGRAMS

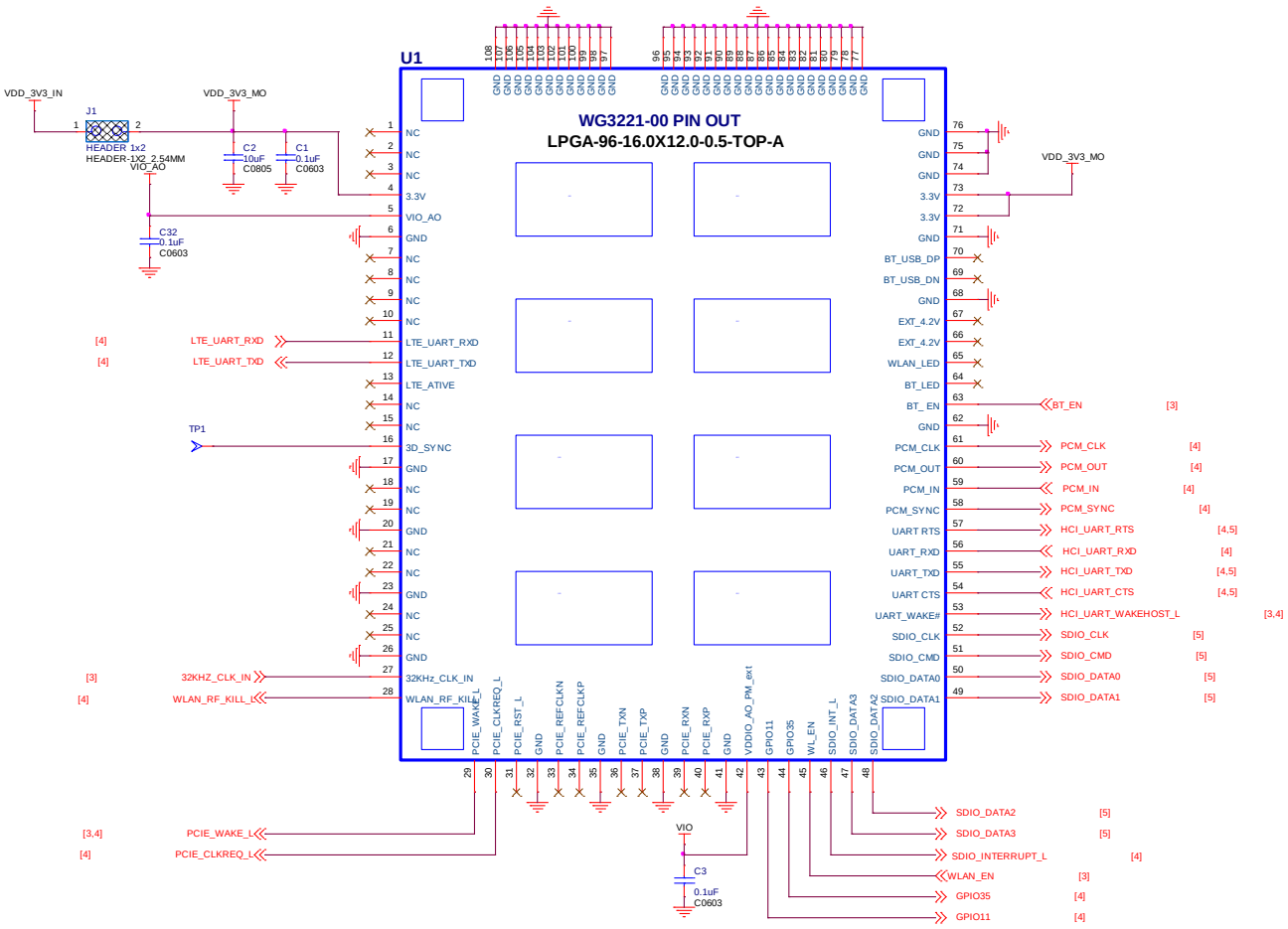


Figure 4-1：WG3221-00 module

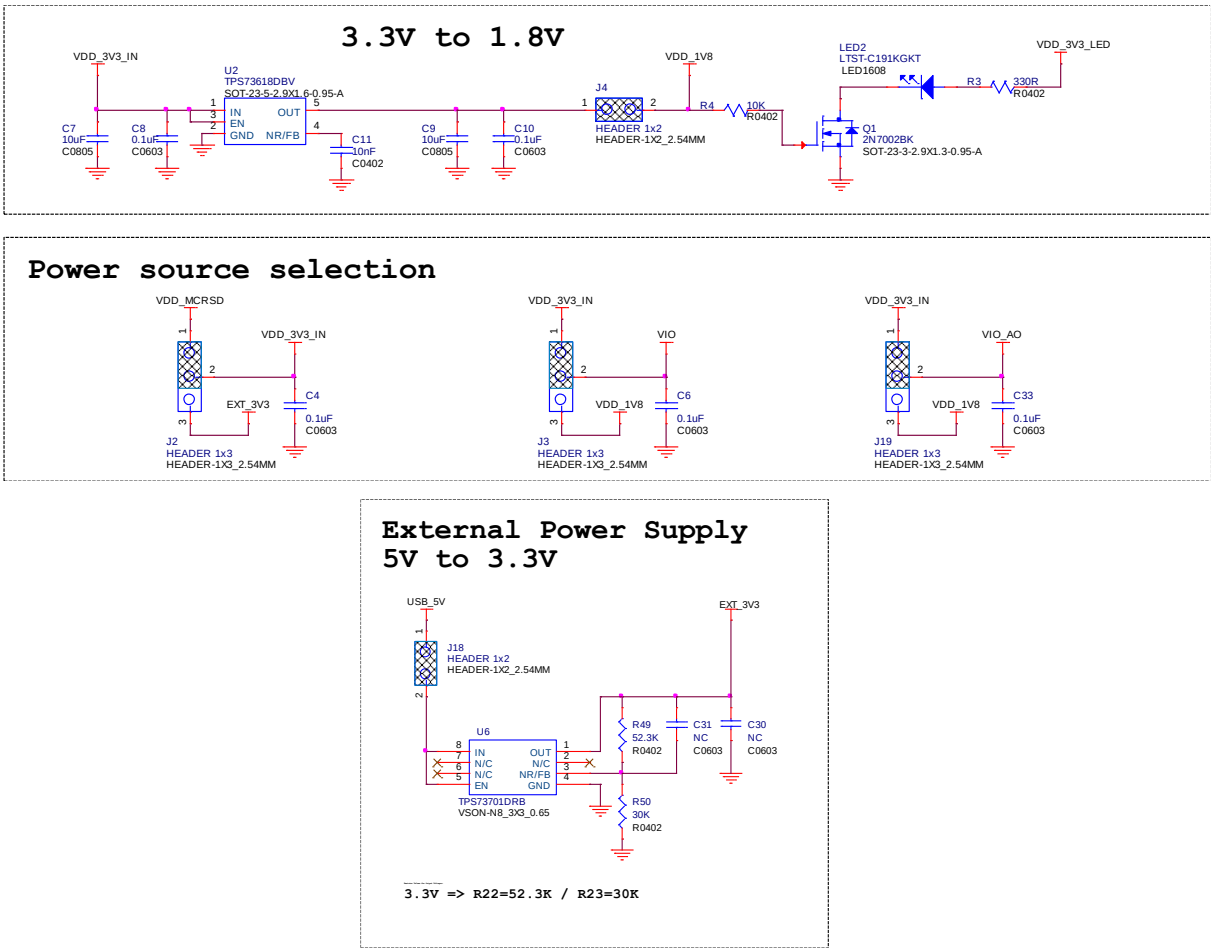
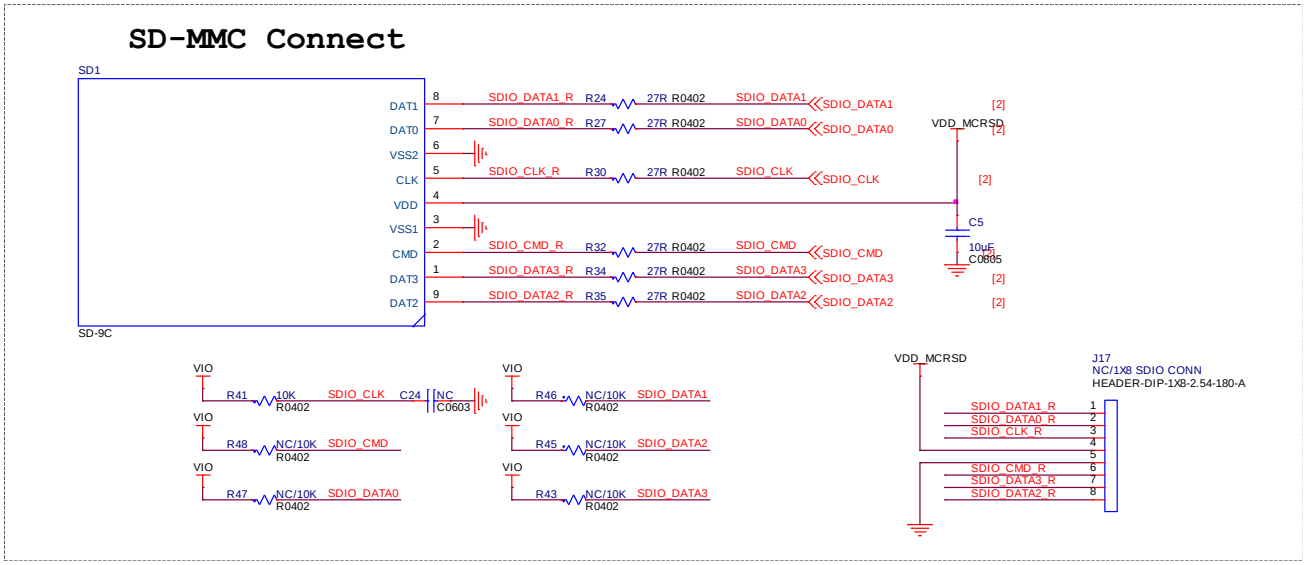


Figure 4-2：Power Circuit



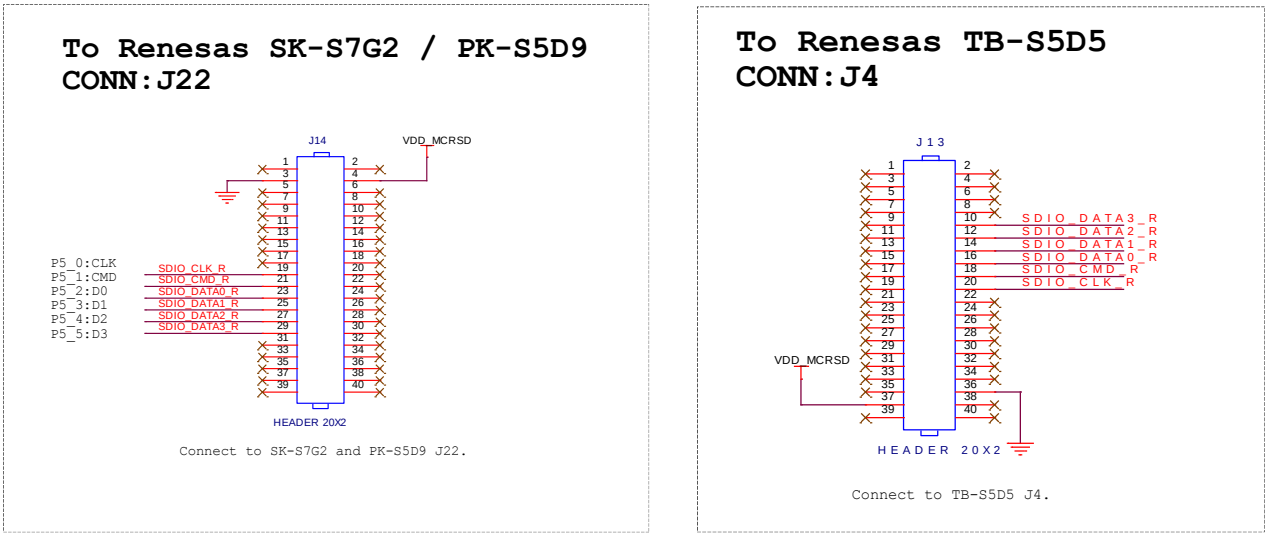


Figure 4-3：SDIO interface

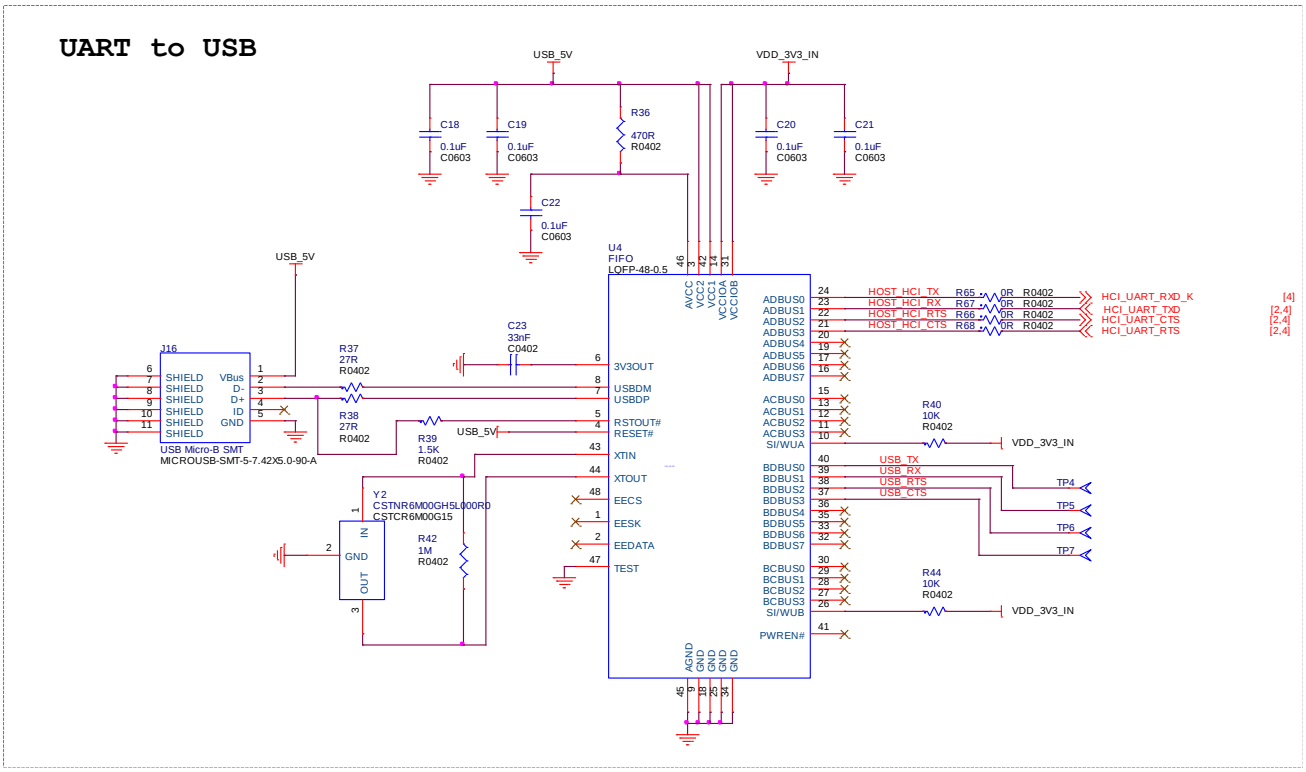


Figure 4-4：UART to USB

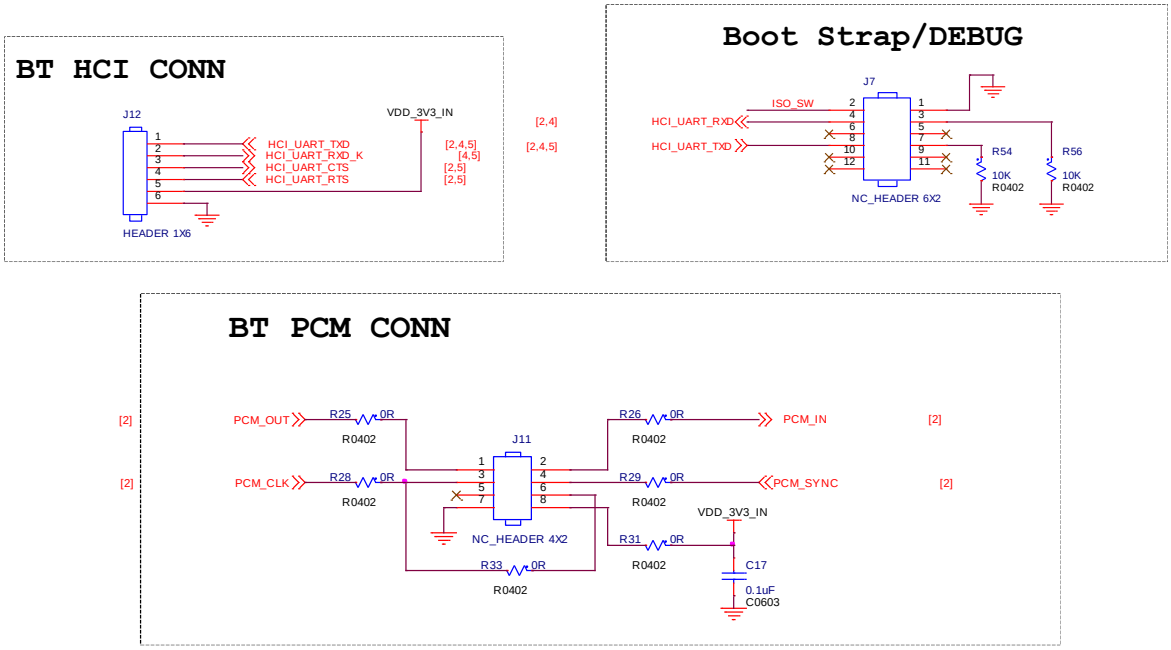


Figure 4-5：HCI UART and PCM/I2S interface

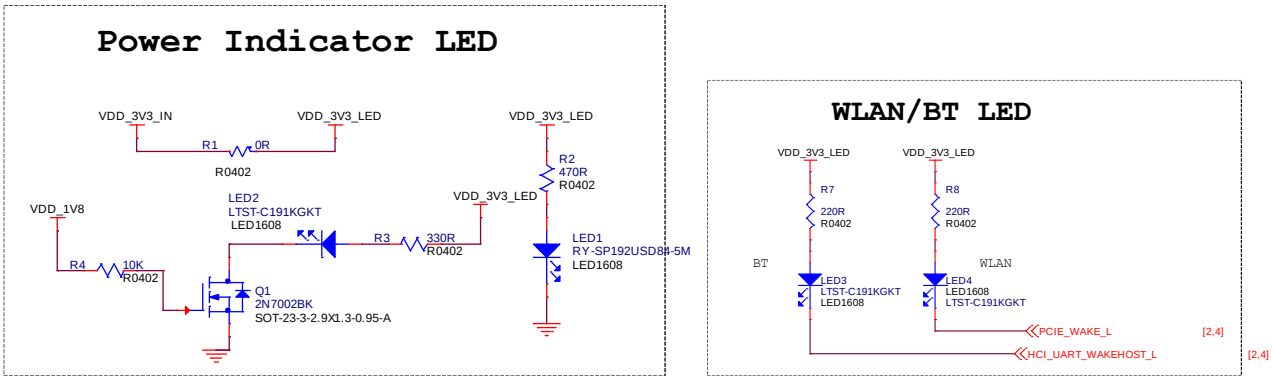


Figure 4-6：LEDs Circuit

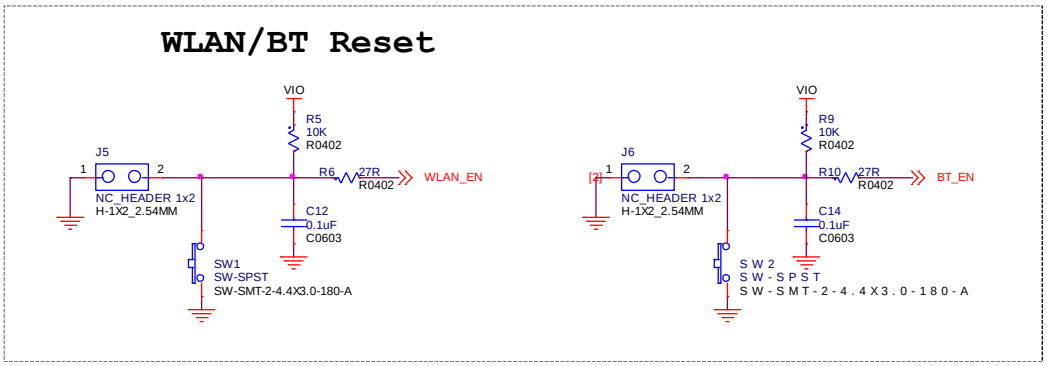


Figure 4-7：WLAN/BT reset and off

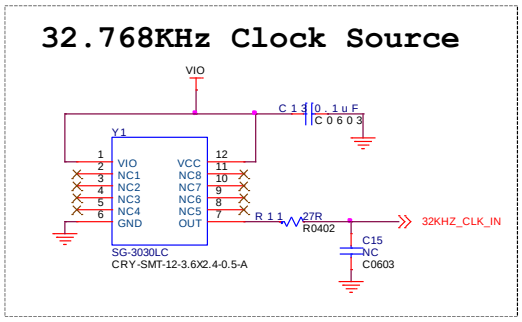
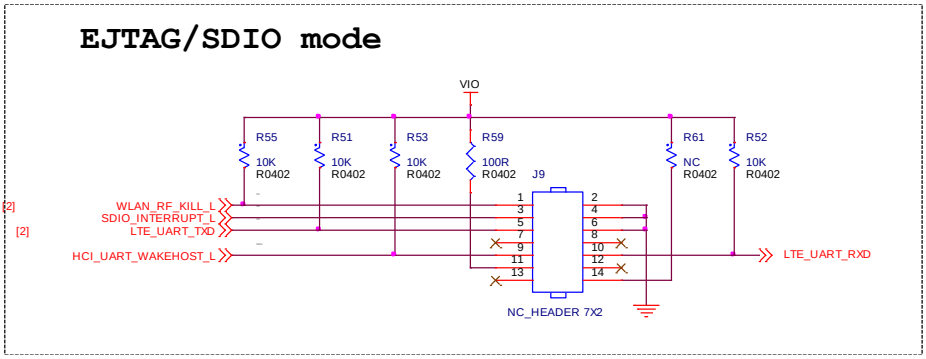


Figure 4-8：32.768KHz Clock source



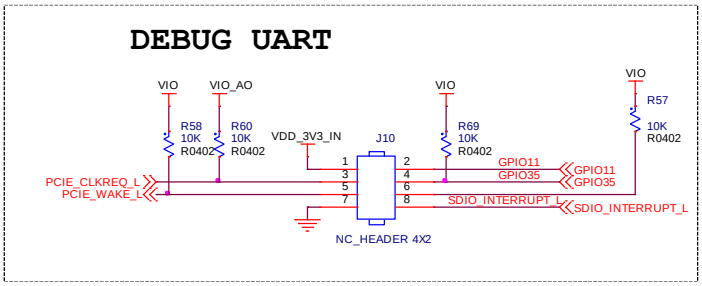


Figure 4-9：Debug CONN

5. HISTORY CHANGE

Revision	Date	Description
D 0.1	2019.01.16	Draft release
D 0.2	2019.06.20	1. Update EVB board drawing in Section 2.1 2. Add VIO_AO description in Section 2. 3. Add platform connection information in Section 3.