SX9330

PerSe™ Connect, High Performance 4-ch. SAR Sensor

WIRELESS & SENSING PRODUCTS

Features

- 2.7-3.6V Input Supply Voltage
- Up to 4 Capacitive Sensor Inputs
  - Patented On-Chip Smart Engine For SAR
  - Capacitance Resolution down to 1aF
  - Capacitance Offset Compensation up to 300pF
  - Multiple thresholds per sensing input
  - Separate configurations per input
- Automatic Calibration
- Up to 2 LED Drivers
  - Up to 20mA Sink Current per IO
  - Intensity Control (256-step PWM)
- Ultra-Low Power Consumption
  - Active Mode: 27 uA
  - Doze Mode: 7 uA
  - Sleep Mode: 1.1 uA
- I2C Serial Interface
  - 2 Sub-Addresses Selectable by Pin
- Programmable Interrupt or Real-Time Status Pin
- -40°C to +85°C Operation
- Compact Size Packages
  - 1.60 x 1.90 mm DFN
  - 1.25 x 1.26 mm WLCSP
- Pb & Halogen Free, RoHS/WEEE compliant

Applications

- Mobile Phones
- Tablets
- Notebooks
- Wearables

Description

The SX9330 is a 4-channel smart capacitive sensor for SAR (Specific Absorption Rate) applications with an LED driver.

The integrated Smart Engine has a unique feature to accurately discriminate between an inanimate object and human body to enhance SAR applications.

In portable electronic devices, the resulting detection is used to reduce and control radio frequency (RF) emission power in the presence of a human body, enabling significant performance advantages for manufacturers of electronic devices with electro-magnetic radiation sources to meet stringent emission regulations' criteria and Specific Absorption Rate (SAR) standards.

Operating directly from an input supply voltage of 2.7-3.6V, the SX9330 outputs its data via I2C serial bus. The I2C serial communication bus port is compatible with 1.8V host control to report body detection/proximity and to facilitate parameter settings adjustment. Upon proximity detection, the NIRQ output asserts, enabling the user to either determine the relative proximity distance, or simply obtain an indication of detection.

The SX9330 includes an on-chip auto-calibration controller that regularly performs sensitivity adjustments to maintain peak performance over a wide variation of temperature, humidity and noise environments, providing simplified product development and enhanced performance.

Typical Application Circuit

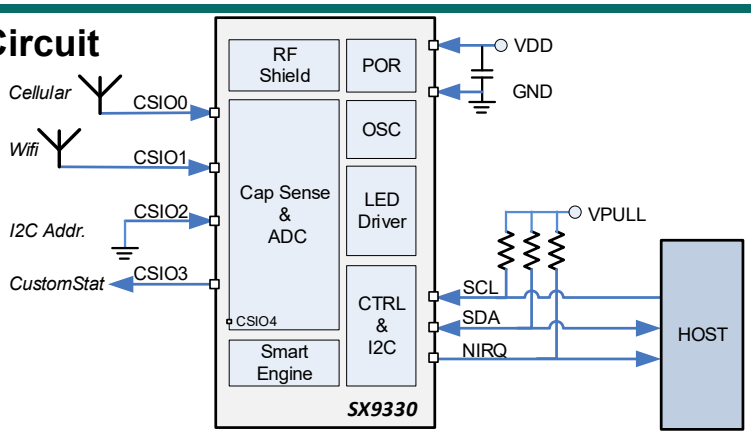


Table of Contents

Ordering Information

Part Number	Package	Marking
SX9330IULTRT[1]	DFN-8	AJ5
SX9330ICSTRT[1]	WLCSP-9	RM2
SX9330EVKA	Eval. Kit for DFN	-
SX9330EVKB	Eval. Kit for WLCSP	-

[1] 3000 Units/reel

Table 1: Ordering Information

1. General Description

1.1. Pin Diagram

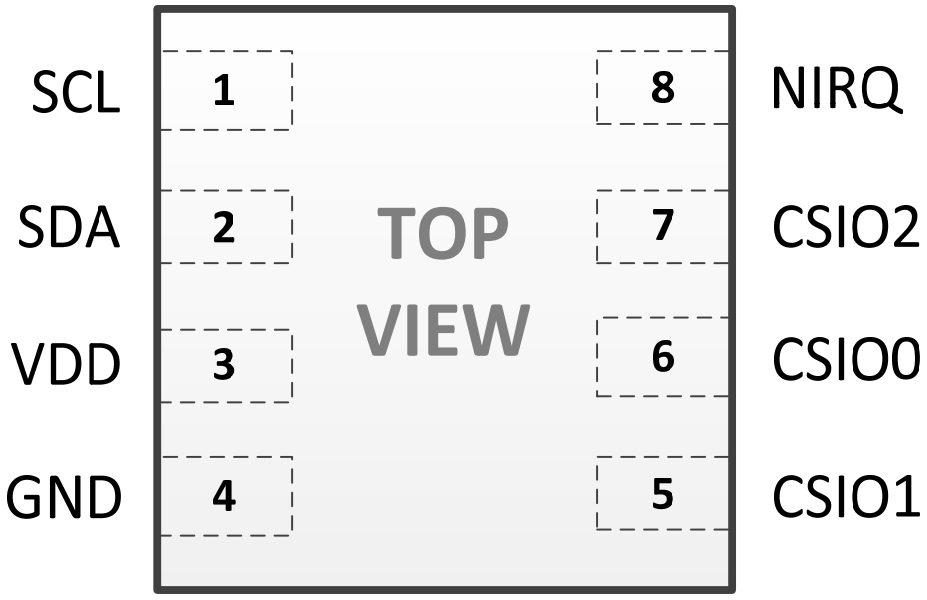


Figure 1: Pin Diagram – DFN Package

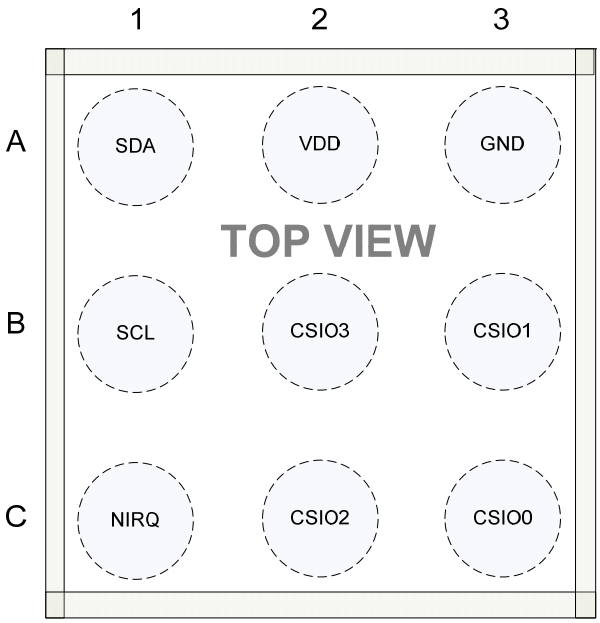
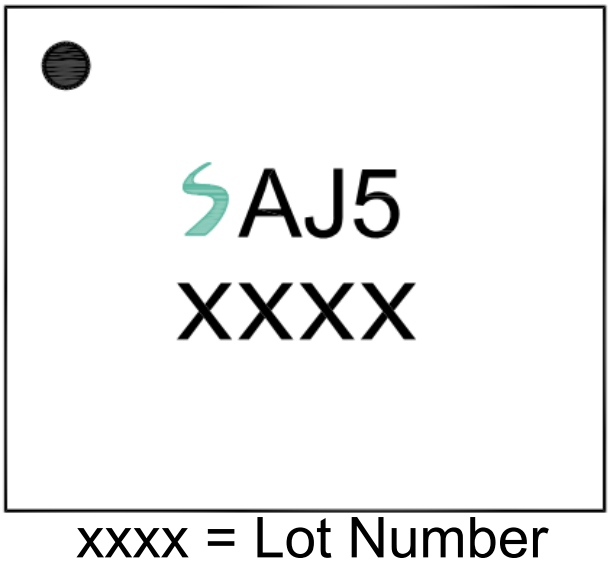


Figure 2: Pin Diagram – WLCSP Package

1.2. Marking Information



xxxx = Lot Number

Figure 3: Marking Information – DFN Package

xxxx = Lot Number

Figure 4: Marking Information – WLCSP Package

1.3. Pin Description

Name	Type	Description
VDD	Power	Power Supply, requires decoupling capacitor.
GND	Ground	Ground.
CSIO0	Analog/Digital	Capacitive Sensor Input/Shield OR Digital I/O OR Analog Input.
CSIO1	Analog/Digital	Capacitive Sensor Input/Shield OR Digital I/O OR Analog Input.
CSIO2	Analog/Digital	Capacitive Sensor Input/Shield OR Digital I/O OR Analog Input OR I2C Sub-Address Input.
CSIO3*	Analog/Digital	Capacitive Sensor Input/Shield OR Digital I/O OR Analog Input.
CSIO4**	Analog/Digital	Capacitive Sensor Input/Shield OR Digital I/O OR Analog Input.
SCL	Digital Input	I2C Clock, requires pull-up resistor.
SDA	Digital Input/Output	I2C Data, requires pull-up resistor.
NIRQ	Digital Input/Output	Interrupt Output OR Digital Input/Output, requires pull-up resistor.

* Not bonded-out in DFN package.

** Not balled/bonded-out both in DFN and WLCSP packages.

Table 2: Pin Description

2. Electrical Characteristics

2.1. Absolute Maximum Ratings

Stresses above the values listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these, or any other conditions beyond the "Operating Conditions", is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability and proper functionality.

Parameter		Symbol	Min	Max	Unit
Supply Voltage		VDD	-0.5	3.9	V
Input Voltage (non-supply pins)		V_{IN}	-0.5	3.9	
Input Current Per Pin (non-supply pins)		I_{IN}	-50	50	mA
Total Input Current (non-supply pins)		I_{INTOT}	-300	300	
Operating Junction Temperature		T_{JCT}	-40	125	°C
Reflow Temperature		T_{RE}	-	260	
Storage Temperature		T_{STOR}	-50	150	
ESD CDM		ESD_{CDM}	1	-	kV
ESD HBM (ANSI/ESDA/JEDEC JS-001)	CSIOx pins	$ESD_{HBMCSIO}$	8	-	kV
	Other pins	ESD_{HBMOTH}	4	-	

Table 3: Absolute Maximum Ratings

2.2. Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	2.7	3.6	V
Pull-up Voltage	V_{PULL}	1.6	3.6	V
Ambient Temperature	T_A	-40	85	°C

Table 4: Operating Conditions

Note: VDD and VPULL (on SCL/SDA/NIRQ) are fully independent, i.e. can be turned ON/OFF separately and in any sequence without creating any leakage current.

2.3. Thermal Characteristics

Parameter	Symbol	Typical	Unit
Thermal Resistance - Junction to Air (Static Airflow) - DFN	θ_{JADFN}	203	°C/W
Thermal Resistance - Junction to Air (Static Airflow) - WLCSP	θ_{JACSP}	120	°C/W

Table 5: Thermal Characteristics

Note: θ_{JA} is calculated from a package in still air, mounted to 3'' x 4.5'', 4-layer FR4 PCB per JESD51 standards.

2.4. Electrical Specifications

All values are valid within the full operating conditions unless otherwise specified.
Typical values are given for T_A = +25°C, VDD=3.3V unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Current Consumption						
Sleep	I_{SLEEP}	Power down. PHEN = 000000 or chip paused. PWM OFF. I2C listening.	-	1.1	5	uA
Doze	I_{DOZE}	SCANPERIOD = hC8 (~400ms) FREQ = b00110 (~100kHz) RESOLUTION = 64 PHEN = 000001 ADC filt. and Adv. features/engines OFF. PWM OFF. I2C listening. No load.	-	7	15	
Active	I_{ACTIVE}	SCANPERIOD = h0F (~30ms) FREQ = b00110 (~100kHz) RESOLUTION = 64 PHEN = 000001 ADC filt. and Adv. features/engines OFF. PWM OFF. I2C listening. No load.	-	27	48	
Capacitive Sensing Interface						
Measurement Range (Unit Capacitor, Cf. AGAIN)	$C_{RANGEUNIT}$		-	+/-0.55	-	pF
Measurement Resolution	N_{BIT}		-	21	-	bits
	C_{RES}	AGAIN = 0001	-	1	-	aF
Nominal Oscillator Frequency	F_{Osc}		-	4	-	MHz
Oscillator Trim Accuracy	F_{Trim}	Around Nominal Value. T_A = +25°C, VDD = 3.3V.	-4	-	+4	%
Oscillator Temp. Dependency	F_{Temp}	Around Trim Result. Full T_A range, VDD = 3.3V.	-	+/-1	-	%
Oscillator VDD Dependency	F_{VDD}	Around Trim Result. T_A = +25°C, Full VDD range.	-	+/-0.6	-	%
Nominal Sampling Frequencies	F_S	Programmable with FREQ	F_{Osc}/864	-	250	kHz
External DC Cap. to Ground per Measurement Phase	C_{DCEXT}	One CSIOx as measured input.	-	-	300	pF
External Series Resistor per CSIOx Pin	R_{SEREXT}		-	-	2	kΩ
Pre-Charge Input Resistor (Unit Value, Cf. RESFILTIN)	$R_{FILTINUNIT}$		-	2	-	kΩ
Compensation Resistor	$R_{INTUNIT}$		-	125	-	Ω
External Input Voltage Conversion						
Input Range	$V_{INRANGE}$	CSIOx pin	0	-	VDD	V
Output Range	$V_{OUTRANGE}$	PROXUSEFUL	0	-	32767	LSB
Output Slope	$V_{OUTSLOPE}$	PROXUSEFUL	-	32768/VDD	-	LSB/V

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Internal Temperature Sensor Conversion						
Input Range	$T_{INRANGE}$	Ambient Temperature (T_A)	-40	-	85	°C
Output Range	$T_{OUTRANGE}$	PROXUSEFUL	0	-	32767	LSB
Output Slope	$T_{OUTSLOPE}$	PROXUSEFUL	-	58	-	LSB/°C
Digital Input/Output: SCL, SDA, NIRQ, CSIOx						
Input High Voltage	V_{IHCSIO}		0.7*V_{PULL}	-	VDD+0.3[1]	V
	$V_{IHI2CNIRQ}$		0.7*V_{PULL}	-	3.6	
Input Low Voltage	V_{IL}		-0.5	-	0.45	
Input Leakage Current	I_L		-1	-	1	uA
Input Hysteresis	V_{HYS}		0.035	0.15	-	V
Output Low Current (SDA)	I_{OL04}	VOL ≤ 0.32V	3	-	-	mA
	I_{OL06}	VOL ≤ 0.6V	6	-	-	
Output Low Voltage (NIRQ, CSIOx)	V_{OL20}	IOL = 20mA, VDD = 3.3V	-	0.4	1	V
	V_{OL10}	IOL = 10mA, VDD = 3.3V	-	0.2	0.5	V
	V_{OL5}	IOL = 5mA, VDD = 3.3V	-	0.1	0.2	V
Output High Voltage (open-drain mode)	V_{OHCSIO}	From external pull-up or LED.	-	-	VDD+0.3[1]	V
	V_{OHNIRQ}		-	-	3.6	V
Output High Current (push-pull mode)	I_{OHCSIO}	VOH ≥ VDD - 0.4V	3	-	-	mA
CSIO2 external pull-down resistance. (Alternate I2C addr)	$R_{LOWCSIO2}$		-	0	500	Ω
Slew Rate (CSIOx both edges, NIRQ falling edge only)	SR_{00}	30-70%, 100pF load SLEWRATE=00/01/10/11 respectively.	-	2	-	ns
	SR_{01}		-	18	-	
	SR_{10}		-	32	-	
	SR_{11}		-	56	-	
Miscellaneous						
Power-up Time	T_{POR}		-	-	5	ms
Unpause Time	$T_{UNPAUSEC}$	Through unpause Command. From SCL rising edge on bit0 of register RegCmd to PAUSESTAT falling edge.	-	171/F_{Osc}	-	us
	$T_{UNPAUSEI}$	Through Interrupt clearing. From SCL rising edge on bit0 of slave address after restart to PAUSESTAT falling edge.	-	60/F_{Osc}	-	

[1] Without exceeding 3.6V

Table 6: Electrical Specifications

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
I2C Timing Specifications (Cf. figure below)						
SCL clock frequency	f_{SCL}		-	-	400	kHz
SCL low period	t_{LOW}		1.3	-	-	us
SCL high period	t_{HIGH}		0.6	-	-	
Data setup time	$t_{SU;DAT}$		0.1	-	-	
Data hold time	$t_{HD;DAT}$		0	-	-	
Repeated start setup time	$t_{SU;STA}$		0.6	-	-	
Start condition hold time	$t_{HD;STA}$		0.6	-	-	
Stop condition setup time	$t_{SU;STO}$		0.6	-	-	
Bus free time between stop and start	t_{BUF}		1.3	-	-	
Data valid time	$t_{VD;DAT}$		-	-	0.9	
Data valid acknowledge time	$t_{VD;ACK}$		-	-	0.9	
Rise time of SCL and SDA	t_{R400}	Load ≤ 400pF	20	-	300	ns
Fall time of SCL and SDA	t_{F400}	Load ≤ 400pF	20*(V_{PULL} /5.5)	-	300	ns
Input glitch suppression	t_{SP}	Note 1	-	-	50	ns

Note 1: Minimum glitch amplitude is $0.7V_{DD}$ at High level and Maximum $0.3V_{DD}$ at Low level.

Table 7: I2C Timing Specifications

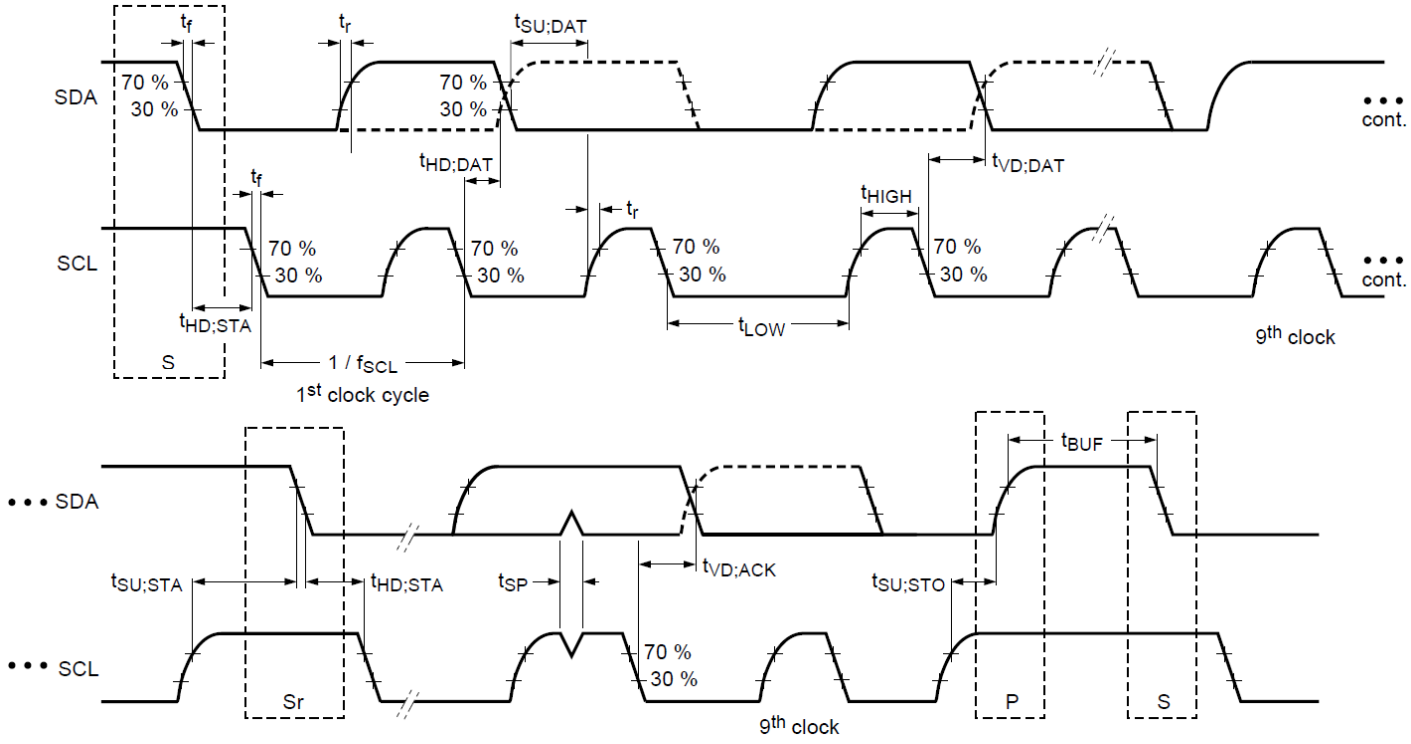


Figure 5: I2C Timing

3. Proximity Sensing Interface

3.1. Introduction

The purpose of the proximity sensing interface is to detect when a conductive object (usually a body part i.e. finger, palm, face, etc) is in the proximity of the system. Note that proximity sensing can be done through the air or through a solid (typically plastic) overlay (also called “touch” sensing).

The chip’s proximity sensing interface is based on capacitive sensing technology. An overview is given the in figure below.

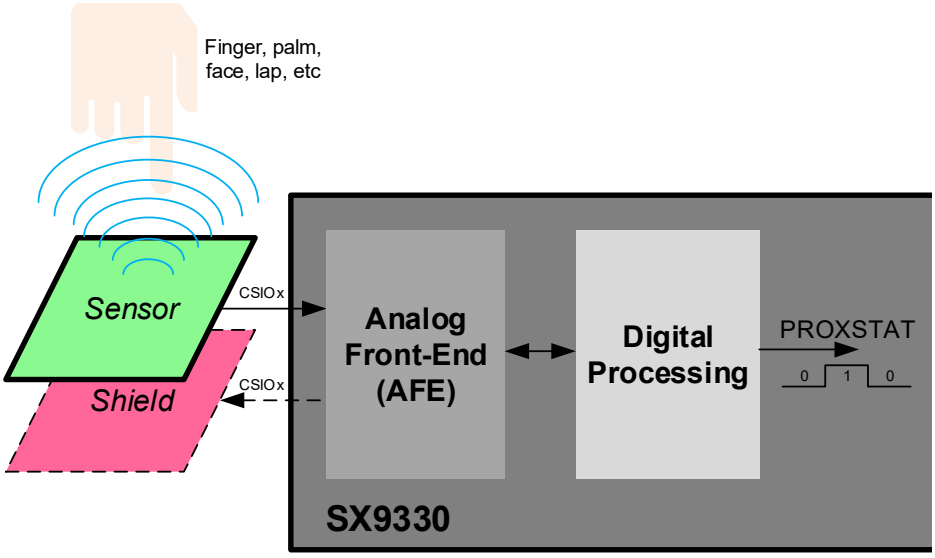


Figure 6: Proximity Sensing Interface Overview

- The sensor can be a simple copper area on a PCB or FPC for example. Its capacitance (to ground) will vary when a conductive object is moving in its proximity.
- The optional shield can also be a simple copper area on a PCB or FPC below/under/around the sensor. It is used to protect the sensor against potential surrounding noise sources and improve its global performance. It also brings directivity to the sensing, for example sensing objects approaching from top only.
- The analog front-end (AFE) performs the raw sensor’s capacitance measurement and converts it into a digital value. It also controls the shield.
- The digital processing block computes the raw capacitance measurement from the AFE and extracts a binary information PROXSTAT corresponding to the proximity status, i.e. object is “Far” or “Close”. It also triggers AFE operations (compensation, etc).

3.2. Scan Period

To save power and since the proximity event is slow by nature, the chip will awake regularly at a programmed scan period (SCANPERIOD) to first sense sequentially each of the enabled phases (PHEN) and then process new proximity samples/info. The chip will then return to an idle mode for the rest of the scan period as illustrated in the figure below.

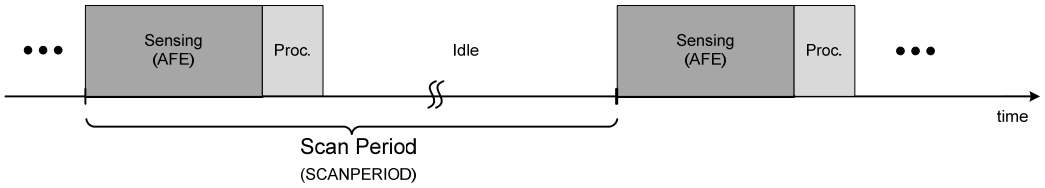


Figure 7: Proximity Sensing Sequencing

The sensing and processing durations vary with the number of phases enabled, the sampling frequency, the resolution programmed, etc. During the Idle state, the chip's analog circuits are turned off. Upon expiry of the idle timer, a new scan period cycle begins.

The scan period determines the minimum reaction time (actual/final reaction time also depends on debounce and filtering settings) and can be programmed from typ. 2ms to 4s.

3.3. Analog Front-End (AFE)

3.3.1. Capacitive Sensing Basics

Capacitive sensing is the art of measuring a small variation of capacitance in a noisy environment. As mentioned above, the chip's proximity sensing interface is based on capacitive sensing technology. In order to illustrate some of the user choices and compromises required when using this technology it is useful to understand its basic principles.

To illustrate the principle of capacitive sensing we will use the simplest implementation where the sensor is a copper plate on a PCB.

The figure below shows a cross-section and top view of a typical capacitive sensing implementation. The sensor connected to the chip is a simple copper area on top layer of the PCB. It is usually surrounded (shielded) by ground for noise immunity (shield function) but also indirectly couples via the ground areas of the rest of the system (PCB ground traces/planes, housing, etc). For obvious reasons (design, isolation, robustness …) the sensor is stacked behind an overlay which is usually integrated in the housing of the complete system.

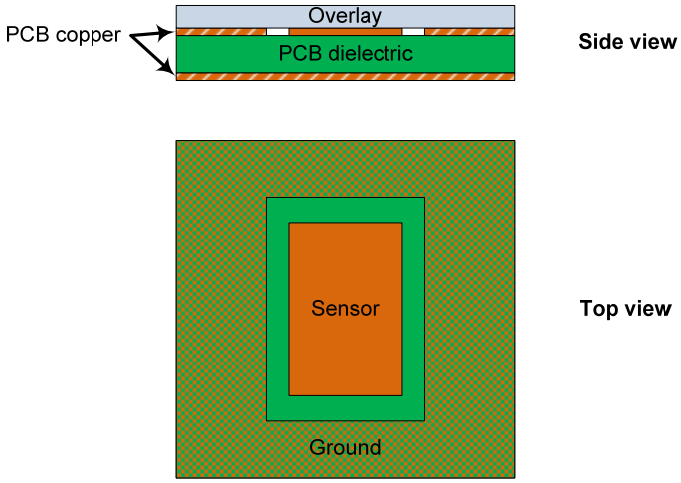


Figure 8: Typical Capacitive Sensing Implementation

When the conductive object to be detected (finger/palm/face, etc) is not present, the sensor only sees an inherent capacitance value C_{Env} created by its electrical field's interaction with the environment, in particular with ground areas.

When the conductive object (finger/palm/face, etc) approaches, the electrical field around the sensor will be modified and the total capacitance seen by the sensor increased by the user capacitance C_{User}. This phenomenon is illustrated in the figure below.

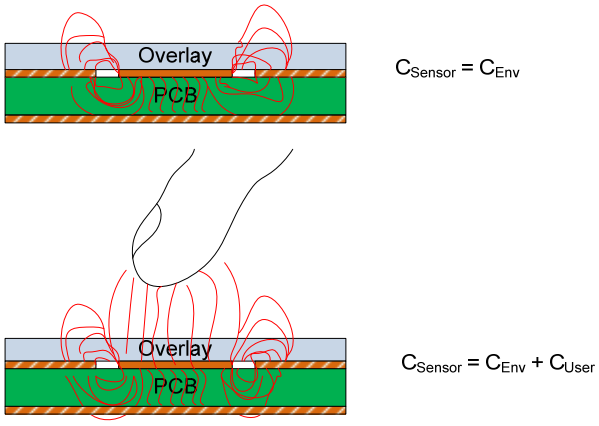


Figure 9: Proximity Effect on Electrical Field and Sensor Capacitance

The challenge of capacitive sensing is to detect this relatively small variation of C_{Sensor} (C_{User} usually contributes for a few percent only) and differentiate it from environmental noise (C_{Env} also slowly varies together with the environment characteristics like temperature, etc). For this purpose, the chip integrates an auto offset compensation mechanism which dynamically monitors and removes the C_{Env} component to extract and process C_{User} only.

In first order, CUser can be estimated by the formula below:

$$C_{User} = \frac{\varepsilon_0 \cdot \varepsilon_r \cdot A}{d}$$

A is the common area between the two electrodes hence the common area between the user's finger/palm/face and the sensor.

d is the distance between the two electrodes hence the proximity distance between the user and the system.

ε_0 is the free space permittivity and is equal to 8.85 10e-12 F/m (constant)

ε_r is the dielectric relative permittivity.

Typical permittivity of some common materials is given in the table below.

Material	Typical ε_r
Glass	8
FR4	5
Acrylic Glass	3
Wood	2
Air	**1**

Table 8: Typical Permittivity of Some Common Materials

From the discussions above we can conclude that the most robust and efficient design will be the one that minimizes C_{Env} value and variations while improving C_{User}.

3.3.2. AFE Block-Diagram

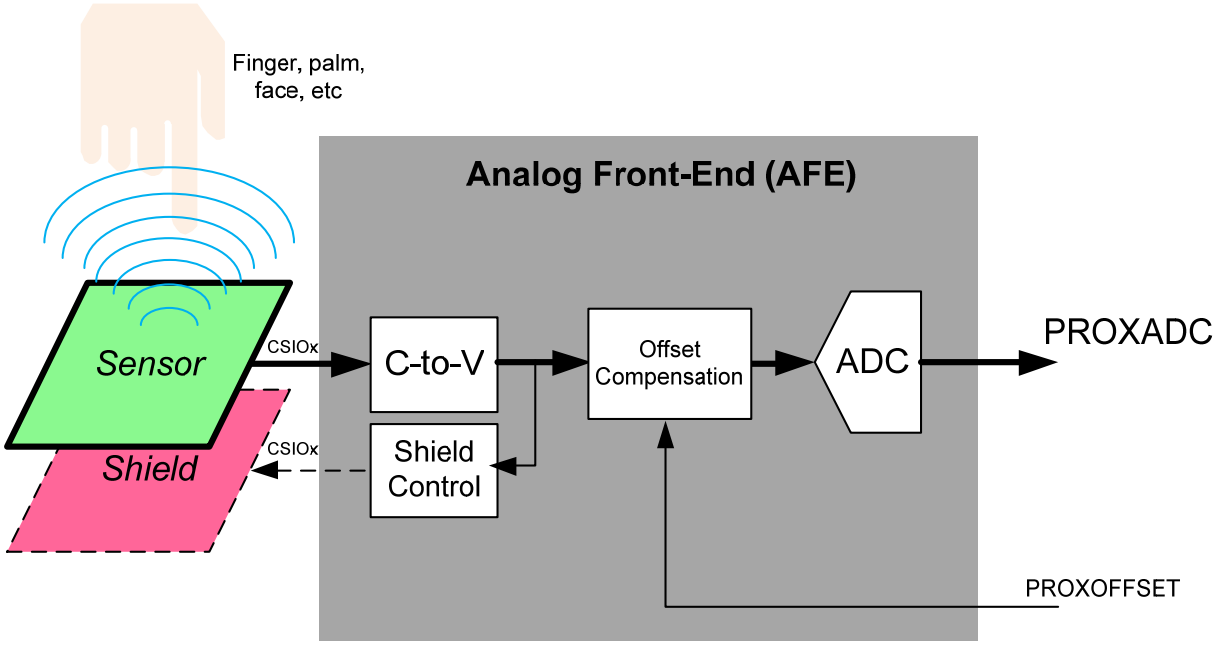


Figure 10: Analog Front-End Block Diagram

3.3.3. Capacitance-to-Voltage Conversion (C-to-V)

The sensitivity of the interface is determined mainly by the AGAIN parameter.
FREQ defines the operating frequency of the interface.

3.3.4. Shield Control

When not being measured, any CSIOx pin can be used as a shield.

3.3.5. Offset Compensation

Offset compensation consists of performing a one-time measurement of C_{Env} and subtracting it from the total capacitance C_{Sensor} in order to feed the ADC with the closest contribution of C_{User} only.

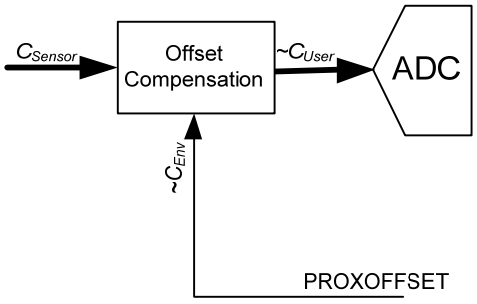


Figure 11: Offset Compensation Block Diagram

The ADC input C_{User} is the total capacitance C_{Sensor} to which C_{Env} is subtracted.

There are three main compensation sources which are illustrated in the figure below. When set to 1, COMPSTAT will only be reset once the compensation is completed.

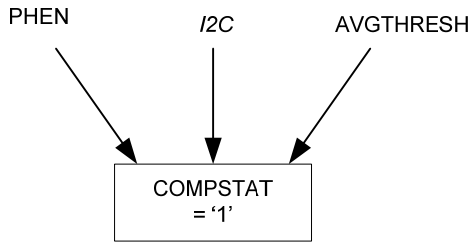


Figure 12: Main Compensation Request Sources

- PHEN: a compensation is automatically requested for a measurement phase on the rising edge of its PHEN bit (needs extra activation command if all PHEN were set to 0).
- I2C: a compensation for one or more phases (enabled thru COMPEN) can be manually requested anytime by the host through I2C interface by issuing the compensation command.
- AVGTHRESH: a compensation for the relevant phase only (or for all, depending on AVGCOMPMETHOD), can be automatically requested if it is detected that C_{Env} has drifted beyond a predefined range programmed by the host.

Note that when compensation occurs, PROXDIFF is reset and hence all compensated phases' PROXSTAT flags turn OFF (i.e. no proximity detected) independently from the user's potential actual presence (except if start-up detection is enabled).

3.3.6. Analog-to-Digital Conversion (ADC)

An ADC is used to convert the analog capacitance information into a digital word PROXADC.

3.4. Digital Processing

3.4.1. Overview

The main purpose of the digital processing block is to convert the raw capacitance information coming from the AFE (PROXADC) into a robust and reliable digital flag (PROXSTAT) indicating if something is within range of the proximity sensor(s).

The offset compensation performed in the AFE is a one-time measurement. However, the environment capacitance C_{Env} may vary with time (temperature, nearby objects, etc). Hence, in order to get the best estimation of C_{User} (PROXDIFF), the digital processing block dynamically tracks and subtracts C_{Env} variations. This is performed by filtering PROXUSEFUL to extract its slow variations (PROXAVG).

PROXDIFF is compared to the user programmable threshold (PROXTHRESH) to extract PROXSTAT flag.

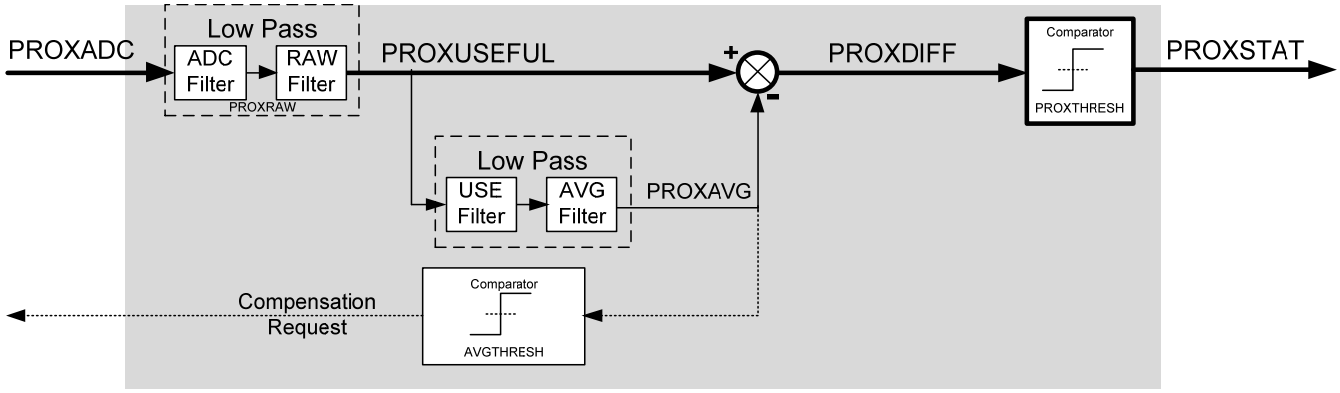


Figure 13: Digital Processing Block Diagram

The digital processor sequence (for all enabled phases) is illustrated below. At every scan period wake-up, the block updates sequentially PROXADC, PROXUSEFUL, PROXAVG, PROXDIFF and PROXSTAT before going back to Idle mode.

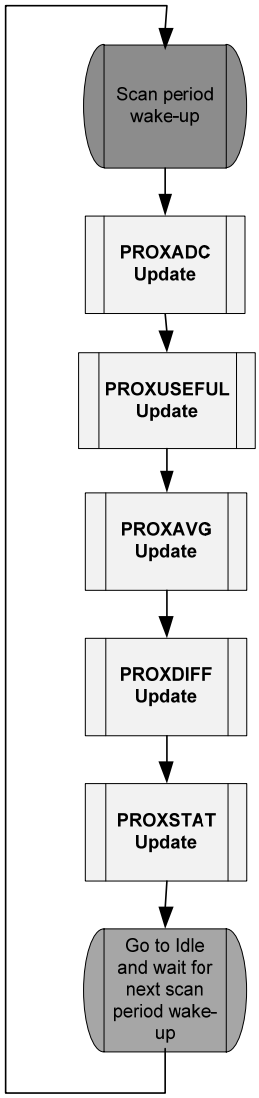


Figure 14: Digital Processor Sequence

The digital processing block also updates COMPSTAT (set when compensation is currently pending execution or completion).

3.4.2. PROXADC Update

PROXADC update consists mainly of starting the AFE and waiting for the new PROXADC values (one for each phase) to be ready. If compensation was pending it is performed first.

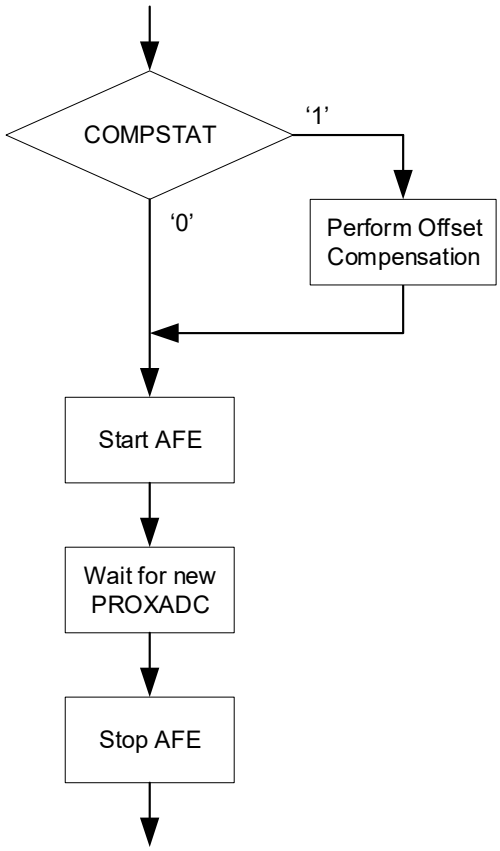


Figure 15: PROXADC Update

Note that PROXADC is not available in the "Main Data Readback" section of the registers. If needed, it can be observed by reading PROXUSEFUL while both ADC and RAW filters are disabled.

3.4.3. PROXUSEFUL Update

PROXUSEFUL update consists of filtering PROXADC, using both ADC and RAW filters, to remove its high frequencies components (system noise, interferer, etc) and extract only user activity (few Hz max) and slow environment changes.

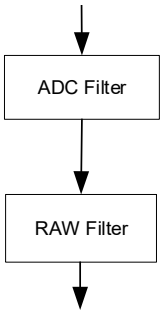


Figure 16: PROXUSEFUL Update

Please refer to the application notes for further details.

3.4.4. PROXAVG Update

PROXAVG update consists of averaging PROXUSEFUL, using both USE and AVG filters, to ignore its “fast” variations (i.e. user finger/palm/hand) and extract only the very slow variations of environment capacitance C_{Env}.

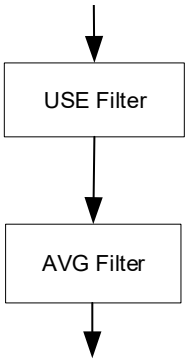


Figure 17: PROXAVG Update

Please refer to the application notes for further details.

3.4.5. PROXDIFF Update

PROXDIFF update consists of the complementary operation i.e. subtracting PROXAVG to PROXUSEFUL to ignore slow capacitances variations (C_{Env}) and extract only user related variations i.e. C_{User}.

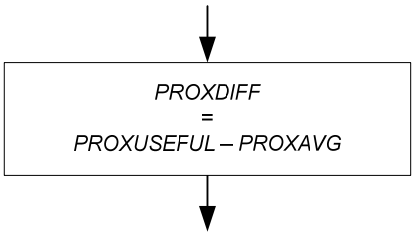


Figure 18: PROXDIFF Update

3.4.6. PROXSTAT Update

PROXSTAT update consists mainly of taking PROXDIFF information (C_{User}), comparing it with a user programmable threshold PROXTHRESH and finally updating PROXSTAT accordingly. When PROXSTAT=1, PROXAVG is typically frozen to prevent the user proximity signal from being absorbed into C_{Env}.

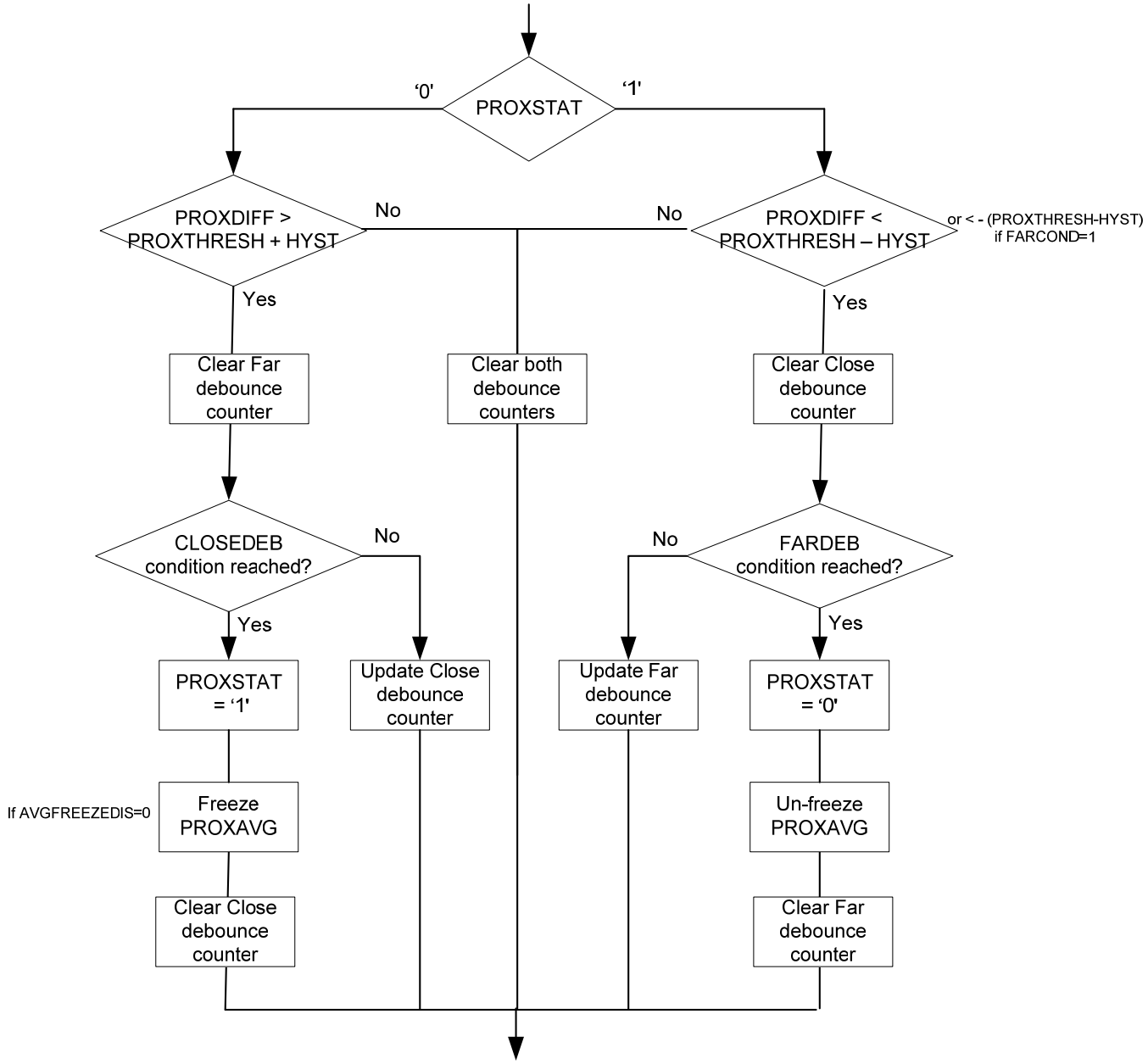


Figure 19: PROXSTAT Update

Please refer to the application notes for further details.

3.5. Host Operation

An interrupt can be triggered when the user is detected as “close” (in range), detected as “far” (out of range), or both (CLOSEANYIRQEN, FARANYIRQEN).

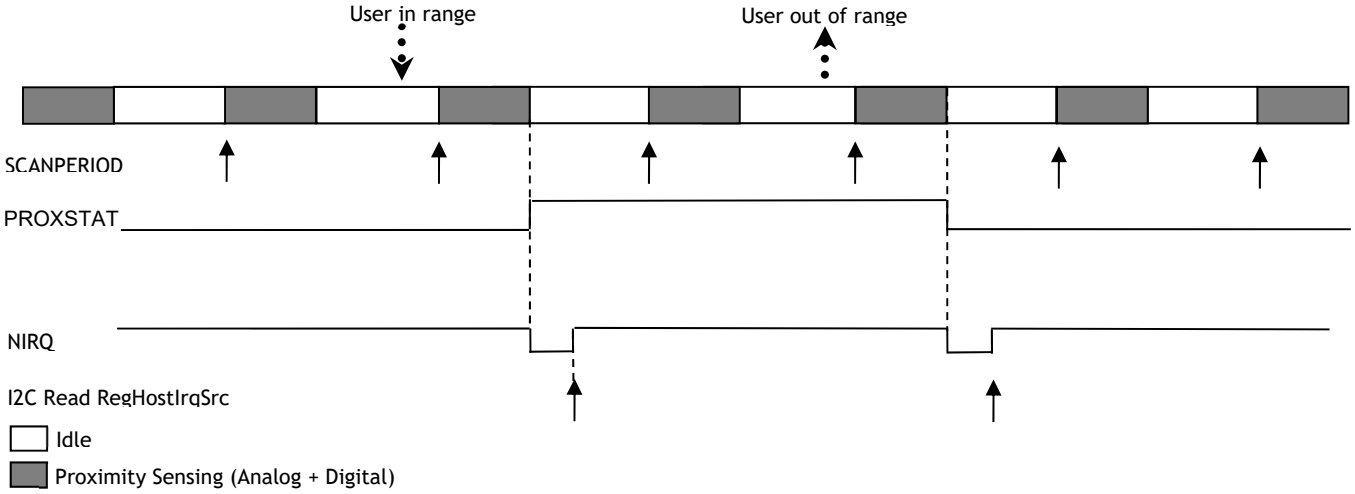


Figure 20: Proximity Sensing Host Operation (Monitoring Close/Far Events)

An interrupt can also be triggered at the end of each scan period’s conversion, indicating to the host when the proximity sensing block is running (CONVDONEIRQEN). This may be used by the host to synchronize noisy system operations or to read phase data (PROXUSEFUL, PROXAVG, and PROXDIFF) synchronously for monitoring purposes.

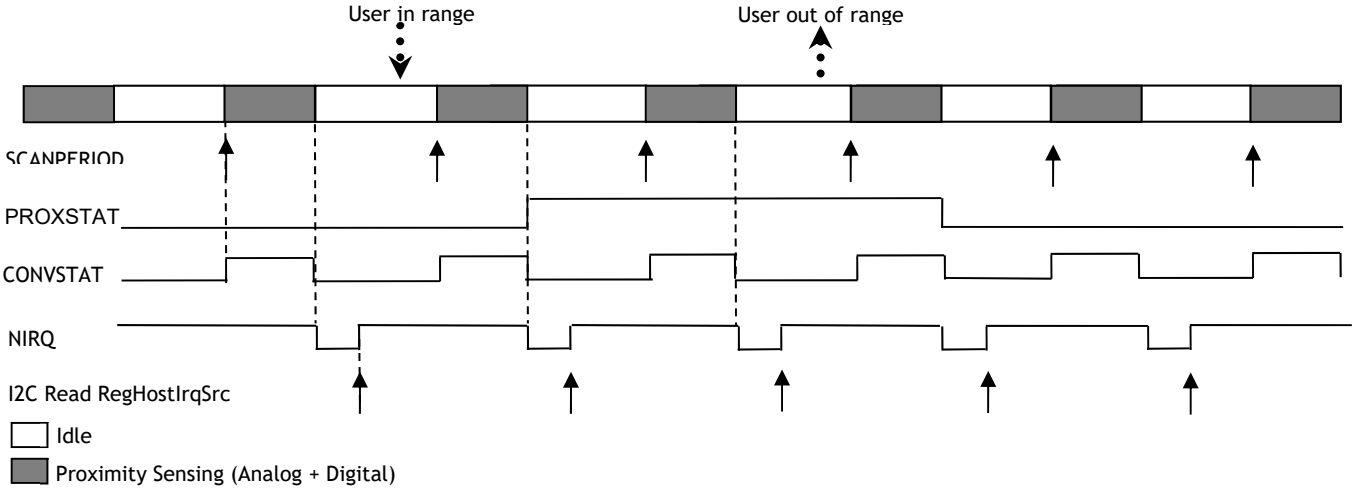


Figure 21: Proximity Sensing Host Operation (Monitoring Conversion Events)

Besides the two examples above, the interrupt can be mapped to many different status bits to accommodate application needs, Cf. register map for the details.

3.6. Operational Modes

3.6.1. Active

Active mode uses fixed and typically short scan periods. All phases can share the same Active scan period (SCANPERIOD) or use different ones as needed (SCANFACTOR_PHx).

3.6.2. Doze

In some applications, the reaction/sensing time needs to be fast when the user is present (proximity detected), but can be slow when no detection has occurred for some time.

The Doze mode, when enabled (DOZEPERIOD), allows the chip to automatically switch between a fast scan period (SCANPERIOD) during proximity detection (by any of the enabled phase) and a slow scan period (DOZEPERIOD) when no proximity is detected. This enables lower average power consumption at the expense of longer reaction times.

After proximity is detected (by any of the enabled phases), the chip will automatically switch to Active mode. And conversely when proximity is not detected anymore (by none of the enable phases), it will automatically switch to Doze mode.

3.6.3. Sleep

Sleep mode can be entered by disabling all phases (PHEN=0). It places the chip in its lowest power mode, with scanning completely disabled and idle period set to continuous. In this mode, only the I2C serial bus is active (and PWM if needed). Enabling any phase (PHEN) and sending activation command will make the chip leave Sleep mode (for Doze if enabled, else Active mode).

Additionally, Sleep mode can also be entered by using the pause feature. However, unlike using PHEN, exiting Sleep mode thru unpause will not generate any compensation. If the pause request is not received during idle, the chip will first complete normally sensing+processing of the enabled phases before entering sleep.

4. I2C Interface

4.1. Introduction

The I2C implemented on the chip and used by the host to interact with it is targeted to comply with:

- Standard (100kb/s) and Fast (400kb/s) modes.
- Slave mode
- 7-bit address
  - Default is 0x28 (b0101000)
  - **Bit 2** will be set if CSIO2 is grounded during reset (power-up or software).
    Important: While CSIO2 is externally grounded, it must be programmed in such a way that it's always set to GND or HZ from the chip.

The host can use the I2C to read and write data at any time, and these changes are effective immediately. Therefore the user may have to disable/enable phases(s) or perform a compensation for new settings to apply properly.

4.2. I2C Read/Write Format

The format of the I2C write and read are given in the figure below. Note that register address is 16-bit and register data is 32-bit.

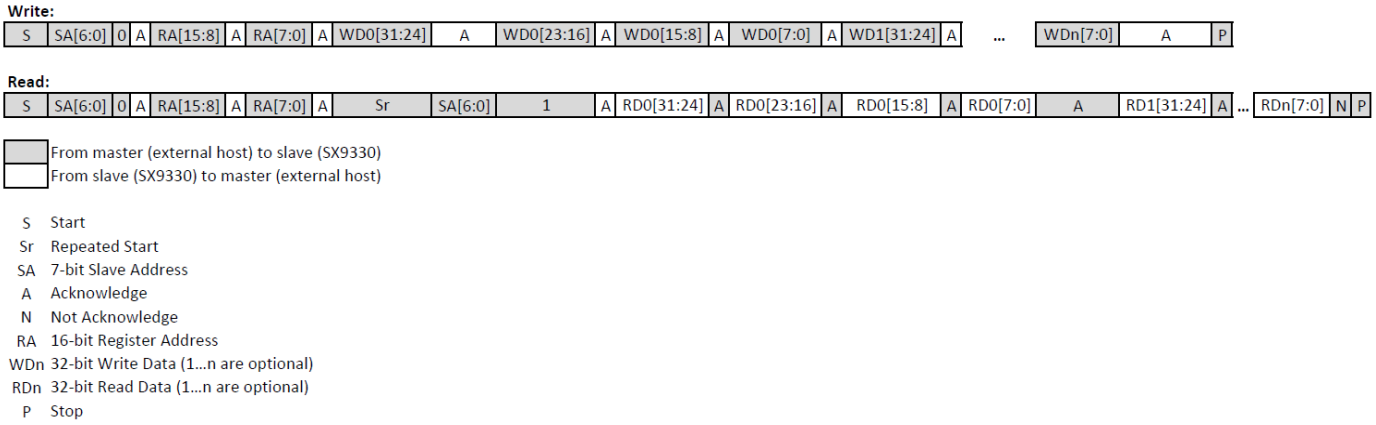


Figure 22: I2C Read/Write Format

The register address is automatically incremented (by 4) when successive register data is supplied (WD1...WDn) or retrieved (RD1...RDn) by the master.

5. Reset

5.1. Power-Up

During a power-up condition, the NIRQ output is (typ.) HIGH until V_{DD} has met its minimum input voltage requirements and a T_{POR} time has expired upon which, NIRQ asserts to a LOW condition indicating that the chip is ready. If needed, the host can perform an I2C read of RegHostIrqSrc to clear this NIRQ status.

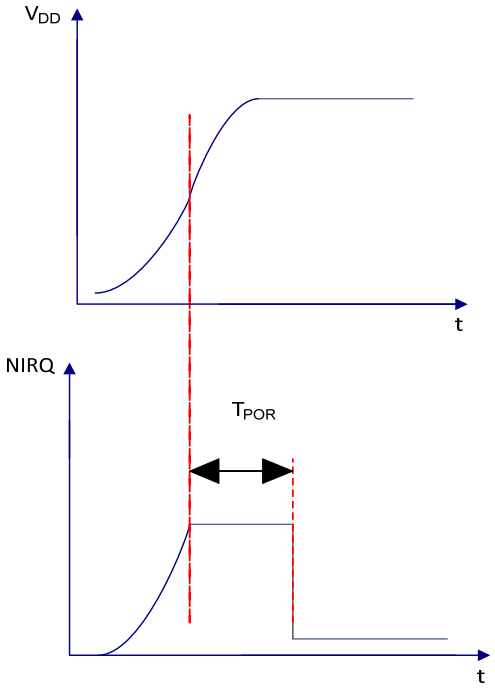


Figure 23: Power-up vs. NIRQ

5.2. Software Reset

The host can also perform a reset anytime by writing 0xDE into RegReset. The NIRQ output will be asserted when the chip is ready and if needed the host can perform an I2C read to clear this NIRQ status.

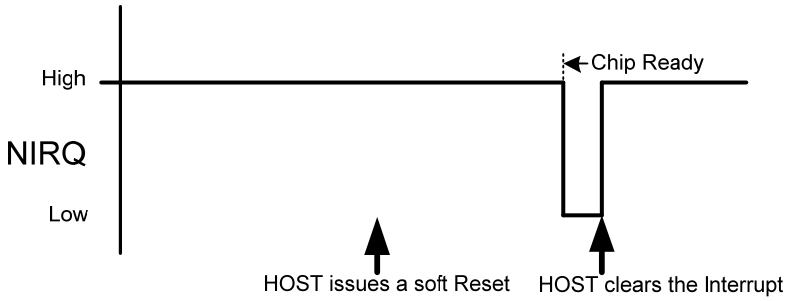


Figure 24: Software Reset

6. Interrupt

6.1. Assertion and Clearing

Except for Reset, the interrupt pin can be asserted once per scan period at the end of the processing phase. It will be automatically cleared after the host performs a read of RegHostIrqSrc (which content will be cleared as well).

7. Registers

The registers below allow the user to do full parameter customization and their values must be set in accordance with the latest application notes available (please contact your Semtech representative).

Please note the following:

a) Addresses not listed are reserved and should not be written.
b) Reserved bits should be left to their default value unless otherwise specified.
c) Unless stated otherwise and when applicable, default values can be considered to be typical ones.

Addr (hex)	Name	Variable	Bits	RW	Default	Description
Interrupt and Pause Control						
4000	RegHostIrqSrc	Reserved	31:8		h000000	
		RESETIRQ	7	R	b1	Reset interrupt source status (i.e. reset occurred).
		CLOSEANYIRQ	6	R	b0	Close interrupt source status (i.e. any PROXSTAT rising edge).
		FARANYIRQ	5	R	b0	Far interrupt source status (i.e. any PROXSTAT falling edge).
		COMPDONEIRQ	4	R	b0	Compensation interrupt source status (i.e. any COMPSTAT falling edge).
		CONVDONEIRQ	3	R	b0	Conversion interrupt source status (i.e. CONVSTAT falling edge).
		PROG2IRQ	2	R	b0	As defined by PROG2IRQCFG.
		PROG1IRQ	1	R	b0	As defined by PROG1IRQCFG.
		PROG0IRQ	0	R	b0	As defined by PROG0IRQCFG.
4004	RegHostIrqMsk	Reserved	31:7		h0000000	
		CLOSEANYIRQEN	6	RW	b1	Enables the close interrupt (any).
		FARANYIRQEN	5	RW	b1	Enables the far interrupt (any).
		COMPDONEIRQEN	4	RW	b0	Enables the compensation interrupt.
		CONVDONEIRQEN	3	RW	b0	Enables the conversion interrupt.
		PROG2IRQEN	2	RW	b0	Enables the PROG2 interrupt.
		PROG1IRQEN	1	RW	b0	Enables the PROG1 interrupt.
		PROG0IRQEN	0	RW	b0	Enables the PROG0 interrupt.
4008	RegHostIrqCtrl	Reserved	31:8		h000000	
		Reserved	7		b0	
		HOSTIRQPINSEL	6	RW	b0	Defines which pin is used as interrupt: b0: NIRQ b1: CSIO4
		HOSTIRQPOLARITY	5	RW	b0	Defines the interrupt pin polarity: b0: Active Low b1: Active High Only applies when HOSTIRQFUNCTION=b0.
		Reserved	4		b0	
		HOSTIRQFUNCTION	3	RW	b0	Disables the interrupt function: b0: On b1: Off
		PAUSEIRQEN	2	RW	b0	Enables pause function via interrupt: b0: Off b1: On, the chip will pause when it sets the interrupt pin active Only applies when HOSTIRQFUNCTION=b0. Note that before going to Sleep(pause) mode, any pending scan period measurements are completed (unlike PHEN). Also, no compensation is performed when Sleep(pause) mode is exited (unlike PHEN).
		PAUSESCOPE	1	RW	b0	Defines the features disabled in Sleep(pause) mode:

						b0: Sensor scanning only b1: Sensor scanning and PWM Engines
		Reserved	0		b0	
4010	RegPauseStat	Reserved	31:1		h00000000	
		PAUSESTAT	0	RW	b0	When set, indicates that the chip is currently in Sleep(pause) mode.
Clock Spreading						
4054	RegAfeCtrl	Reserved	31:18		h0000	
		CLKSPREADRANGE	17	RW	b0	Defines the clock spreading range: b0: Full (16 steps) b1: Reduced (8 steps)
		CLKSPREADEN	16	RW	b0	Enables the sampling frequency clock spreading: b0: Off, fixed sampling frequency as defined by FREQ_PHx b1: On, dynamic sampling frequency automatically varying around FREQ_PHx value at every sampling period Note that this setting applies to all enabled phases and also affects PWM frequency during sensing.
		Reserved	15:0		h0400	
PWM Engines						
4080	RegPwm	PWMLEVELA	31:24	RW	h80	Defines the PWM Engine A duty cycle: h00: 0% Else: PWMLEVELA/255 Default value is ~50%. Note that when enabled, the PROX2PWM engine will force this value accordingly.
		PWMLEVELB	23:16	RW	h80	Same as PWMLEVELA for Engine B.
		Reserved	15		b0	
		PWMSTAGGERING	14	RW	b1	Enables PWM staggering on pins: b0: Off, simultaneous edges b1: On
		PWMENGINESELECT	13:8	RW	b000000	Defines which PWM Engine is mapped to the different pins: b0: Engine A b1: Engine B [13:8]=[NIRQ, CSIO4, CSIO3, CSIO2, CSIO1, CSIO0]
		Reserved	7:2		b000000	
		PWMMASKENABLE	1	RW	b0	Disables PWM Engines during sensor scanning: b0: On, PWM Engines work during sensor scanning b1: Off, PWM Engines levels are fixed to PWMBLOCKEDLEVEL during sensor scanning
		PWMBLOCKEDLEVEL	0	RW	b0	Defines the PWM Engines values during sensor scanning, when PWMMASKENABLE=b1: b0: 0% b1: 100%
4200	RegClkGen	Reserved	31:4		h0000000	
		PWMFREQ	3:0	RW	b1000	Defines the PWM refresh rate: b0000: FOsc /2048 (~1953.12 Hz) b0001: FOsc /4096 (~976.56 Hz) b0010: FOsc /6144 (~651.04 Hz) b0011: FOsc /8192 (~488.28 Hz) b0100: FOsc /10240 (~390.62 Hz) b0101: FOsc /12288 (~325.52 Hz) b0110: FOsc /14336 (~279.01 Hz) b0111: FOsc /16384 (~244.14 Hz) b1000: FOsc /18432 (~217.01 Hz) b1001: FOsc /20480 (~195.31 Hz) b1010: FOsc /22528 (~177.55 Hz) b1011: FOsc /24576 (~162.76 Hz)

						b1100: FOsc /26624 (~150.24 Hz) b1101: FOsc /28672 (~139.50 Hz) b1110: FOsc /30720 (~130.20 Hz) b1111: FOsc /32768 (~122.07 Hz) Cf. FOsc/FTrim/FTemp/FVDD in electrical specifications.
Miscellaneous						
41C4	RegI2cAddr	Reserved	31:7		h0000000	
		I2CADDR	6:0	R	b0101000	Indicates the current I2C address.
4240	RegReset	Reserved	31:8		h000000	
		SOFTRESET	7:0	W	h00	Writing hDE resets the chip.
4280	RegCmd	Reserved	31:4		h0000000	
		COMMAND	3:0	RW	b0000	Writing the following values triggers the corresponding command: b1111: Enables the phases specified by PHEN b1110: Compensates the phases specified by COMPEN b1101: Enters Sleep(pause) mode b1100: Exits Sleep(pause) mode After Command is sent, wait for 1 Scan Period minimum (i.e. Sensing time configured) to allow device change to occur. During command execution, COMMANDBUSY=b1 and no new command should be sent until COMMANDBUSY=b0.
4284	RegTopStat0	Reserved	31:1		h0000000	
		COMMANDBUSY	0	RW	b0	When set, indicates that a command is currently being executed.
Pins Configuration						
42C0	RegPinCfg	Reserved	31:26		b000010	
		PINCFGINEN	25:20	RW	b000000	Enables the input function of the pin: b0: Off b1: On [25:20]=[NIRQ, CSIO4, CSIO3, CSIO2, CSIO1, CSIO0] Note that RegPinCfg defines the behavior of the pins outside of sensing, while during sensing it is defined by RegAfePhPhx.
		PINCFGOUTEN	19:14	RW	b000000	Enables the output function of the pin: b0: Off b1: On [19:14]=[NIRQ, CSIO4, CSIO3, CSIO2, CSIO1, CSIO0] Note that RegPinCfg defines the behavior of the pins outside of sensing, while during sensing it is defined by RegAfePhPhx.
		CSIOCFGSLEWRATE	13:12	RW	b00	Defines the slew rate control for the pins NIRQ and CSIOx: b00: Fastest b01: Fast b10: Slow b11: Slowest This setting applies to both edges for CSIOx and only to the falling edge for NIRQ.
		Reserved	11		b0	
		PINCFGDRIVE	10:6	RW	b00000	Defines the drive type of the corresponding pin: b0: Open-drain b1: Push-pull [10:6]=[CSIO4, CSIO3, CSIO2, CSIO1, CSIO0] Note that this parameter applies only if the corresponding pin is set as output (PINCFGOUTEN=b1).

		PINCFGPWM	5:0	RW	b000000	Enables the PWM function on the corresponding pin: b0: Off b1: On [5:0]=[NIRQ, CSIO4, CSIO3, CSIO2, CSIO1, CSIO0] Note that this parameter applies only if the corresponding pin is set as output (PINCFGOUTEN=b1).
42C4	RegPinDout	Reserved	31:6		h0000000	
		PINDOUT	5:0	RW	b111111	Defines the static output level of the corresponding pin: b0: Low b1: High (HZ if PINCFGDRIVE=b0) [5:0]=[NIRQ, CSIO4, CSIO3, CSIO2, CSIO1, CSIO0] Note that this parameter applies only if the corresponding pin is set as output (PINCFGOUTEN=b1) and PWM is disabled (PINCFGPWM=b0).
42C8	RegPinDin	Reserved	31:6		h0000000	
		PINDIN	5:0	R	b111111	Indicates the static input level of the corresponding pin: b0: Low b1: High [5:0]=[NIRQ, CSIO4, CSIO3, CSIO2, CSIO1, CSIO0] Note that this bit reads 1 if the corresponding pin is not set as input (PINCFGINEN=b0).
Chip Information						
42D8	RegInfo	Reserved	31:16		h0000	
		WHOAMI	15:8	R	h30	Chip Identification Number.
		REVISION	7:0	R	h17	Chip Revision.
Status Bits						
8000	RegStat0	Reserved	31:30		b00	
		PROXSTAT	29:24	R	b000000	Indicates if proximity is currently being detected for corresponding phase (i.e. set when phase's PROXDIFF value is above detection threshold, Cf. FARCOND for clearing). [29:24]=[PH5, PH4, PH3, PH2, PH1, PH0]
		Reserved	23:22		b00	
		TABLESTAT	21:16	R	b000000	When PROXSTAT=b1 (ignoring STEADYCOND_PHx impact), indicates if the object detected by the current phase is currently being recognized as a table (i.e. sensor within TABLETHRESH_PHx; HYST_PHx and CLOSE/FARDEB_PHx apply). When PROXSTAT=b0 (ignoring STEADYCOND_PHx impact), forced to b0. [21:16]=[PH5, PH4, PH3, PH2, PH1, PH0]
		Reserved	15:14		b00	
		BODYSTAT	13:8	R	b000000	When PROXSTAT=b1 (ignoring STEADYCOND_PHx impact), indicates if the object detected by the current phase is currently being recognized as a human body (i.e. phase exceeds BODYTHRESH_PHx, HYST_PHx and CLOSE/FARDEB_PHx apply). When PROXSTAT=b0 (ignoring STEADYCOND_PHx impact), forced to b0. [13:8]=[PH5, PH4, PH3, PH2, PH1, PH0]
		Reserved	7:6		b00	

		STEADYSTAT	5:0	R	b000000	Indicates if the Diff (or Useful, Cf. STEADYEN_PHx) value of the corresponding phase is currently steady (i.e. set when value varied by max STEADYMAXVAR_PHx LSBs (peak-peak) within the last STEADYDEB_PHx sliding window; Cf. UNSTEADYDEB_PHx for clearing). [5:0]=[PH5, PH4, PH3, PH2, PH1, PH0]
8004	RegStat1	Reserved	31:30		b00	
		FAILSTAT	29:24	R	b000000	Indicates if a failure (abnormal PROXOFFSET_PHx value, Cf. FAILTHRESH_PHx) has been detected in the current scan period for the corresponding phase. [29:24]=[PH5, PH4, PH3, PH2, PH1, PH0]
		Reserved	23:22		b00	
		COMPSTAT	21:16	R	b000000	Indicates if compensation is currently pending/running for the corresponding phase. [21:16]=[PH5, PH4, PH3, PH2, PH1, PH0]
		Reserved	15:14		b00	
		SATSTAT	13:8	R	b000000	Indicates if saturation (i.e. Useful exceeds SATTHRESH_PHx) is currently being detected for the corresponding phase. [13:8] = [PH5, PH4, PH3, PH2, PH1, PH0] Note that flag is not automatically cleared when feature is disabled.
		CONVSTAT	7	R	b0	Indicates if new data is currently being measured (set between the beginning of a scanperiod and the end of the last phase measurement).
		STEPSTATB	6	R	b0	Indicates if a step is currently being detected by Engine B. Note that flag is not automatically cleared when feature is disabled.
		STEPSTATA	5	R	b0	Indicates if a step is currently being detected by Engine A. Note that flag is not automatically cleared when feature is disabled.
		STARTUPSTATANY	4	R	b0	Indicates if any of the STARTUPSTAT bits is currently set.
		Reserved	3		b0	
		FAILSTATANY	2	R	b0	Indicates if any of the FAILSTAT bits is currently set.
		STEADYSTATALL	1	R	b0	Indicates if all enabled phases are currently steady.
		PROXSTATANY	0	R	b0	Indicates if any of the PROXSTAT bits is currently set.
8008	RegStat2	Reserved	31:10		h000000	
		CUSTOMSTATB	9	R	b0	Indicates the current output value of the CustomStat engine B (see CUSTOMOUT_ENGB).
		CUSTOMSTATA	8	R	b0	Indicates the current output value of the CustomStat engine A (see CUSTOMOUT_ENGA).
		Reserved	7:6		b00	
		STARTUPSTAT	5:0	R	b000000	Indicates if start-up detection is forcing PROXSTAT=b1 for the corresponding phase. [5:0]=[PH5, PH4, PH3, PH2, PH1, PH0]
CustomStat Engines						
800C	RegIrqCfg0	CUSTOMSTATEN_ENGB	31	RW	b0	Enables CustomStat engine B: b0: Off b1: On, CUSTOMSTATB is generated accordingly.
		CUSTOMSTATEN_ENGA	30	RW	b0	Enables CustomStat engine A: b0: Off b1: On, CUSTOMSTATA is generated accordingly.
		Reserved	29:24		b000000	

		FAILCOND	23	RW	b0	Enables fail condition for status flags: b0: Off b1: While any FAILSTAT bit is set, PROX/BODY/TABLE statuses for that phase are respectively set to b1/b1/b0 independently from their current value.
		COMPSATIRQDIS	22	RW	b0	Disables Compensation interrupt (COMPSTAT not cleared) if PROXOFFSET is saturated.
		PROG2IRQCFG	21:20	RW	b00	Defines the source of PROG2IRQ: b00: Any BODYSTAT/TABLESTAT rising or falling edge b01: Reserved b10: CONVSTAT falling edge b11: CUSTOMSTATA rising or falling edge
		PROG1IRQCFG	19:18	RW	b00	Defines the source of PROG1IRQ: b00: Any STEADYSTAT rising or falling edge b01: Any STEADYSTAT rising edge b10: Any STEADYSTAT falling edge b11: STEADYSTATALL rising or falling edge
		PROG0IRQCFG	17:16	RW	b00	Defines the source of PROG0IRQ: b00: Any FAILSTAT rising or falling edge b01: STARTUPSTATANY rising or falling edge b10: Any SATSTAT rising or falling edge b11: Any STEPSTAT rising edge
		CUSTOMINAREG_ENGA	15:12	RW	b0000	Defines the input sub-register A of CustomStat engine A: b0000: PROXSTAT b0001: TABLESTAT b0010: BODYSTAT b0011: STEADYSTAT b0100: FAILSTAT b0101: COMPSTAT b0110: SATSTAT b0111: RegStat1[7:0] b1000: STARTUPSTAT
		Reserved	11		b0	
		CUSTOMINABIT_ENGA	10:8	RW	b000	Defines the input bit A of CustomStat engine A: b000: bit 0 of register selected by CUSTOMINAREG_ENGA b001: bit 1 of register selected by CUSTOMINAREG_ENGA b010: bit 2 of register selected by CUSTOMINAREG_ENGA b011: bit 3 of register selected by CUSTOMINAREG_ENGA b100: bit 4 of register selected by CUSTOMINAREG_ENGA b101: bit 5 of register selected by CUSTOMINAREG_ENGA b110: bit 6 of register selected by CUSTOMINAREG_ENGA b111: bit 7 of register selected by CUSTOMINAREG_ENGA
		CUSTOMINBREG_ENGA	7:4	RW	b0000	Defines the input sub-register B of CustomStat engine A: b0000: PROXSTAT b0001: TABLESTAT b0010: BODYSTAT b0011: STEADYSTAT b0100: FAILSTAT b0101: COMPSTAT b0110: SATSTAT

						b0111: RegStat1[7:0] b1000: STARTUPSTAT
		Reserved	3		b0	
		CUSTOMINBBIT_ENGA	2:0	RW	b000	Defines the input bit B of CustomStat engine A: b000: bit 0 of register selected by CUSTOMINBREG_ENGA b001: bit 1 of register selected by CUSTOMINBREG_ENGA b010: bit 2 of register selected by CUSTOMINBREG_ENGA b011: bit 3 of register selected by CUSTOMINBREG_ENGA b100: bit 4 of register selected by CUSTOMINBREG_ENGA b101: bit 5 of register selected by CUSTOMINBREG_ENGA b110: bit 6 of register selected by CUSTOMINBREG_ENGA b111: bit 7 of register selected by CUSTOMINBREG_ENGA
8010	RegIrqCfg1	CUSTOMINCREG_ENGA	31:28	RW	b0000	Defines the input sub-register C of CustomStat engine A: b0000: PROXSTAT b0001: TABLESTAT b0010: BODYSTAT b0011: STEADYSTAT b0100: FAILSTAT b0101: COMPSTAT b0110: SATSTAT b0111: RegStat1[7:0] b1000: STARTUPSTAT
		Reserved	27		b0	
		CUSTOMINCBIT_ENGA	26:24	RW	b000	Defines the input bit C of CustomStat engine A: b000: bit 0 of register selected by CUSTOMINCREG_ENGA b001: bit 1 of register selected by CUSTOMINCREG_ENGA b010: bit 2 of register selected by CUSTOMINCREG_ENGA b011: bit 3 of register selected by CUSTOMINCREG_ENGA b100: bit 4 of register selected by CUSTOMINCREG_ENGA b101: bit 5 of register selected by CUSTOMINCREG_ENGA b110: bit 6 of register selected by CUSTOMINCREG_ENGA b111: bit 7 of register selected by CUSTOMINCREG_ENGA
		CUSTOMINDREG_ENGA	23:20	RW	b0000	Defines the input sub-register D of CustomStat engine A: b0000: PROXSTAT b0001: TABLESTAT b0010: BODYSTAT b0011: STEADYSTAT b0100: FAILSTAT b0101: COMPSTAT b0110: SATSTAT b0111: RegStat1[7:0] b1000: STARTUPSTAT
		Reserved	19		b0	

		CUSTOMINDBIT_ENGA	18:16	RW	b000	Defines the input bit D of CustomStat engine A: b000: bit 0 of register selected by CUSTOMINDREG_ENGA b001: bit 1 of register selected by CUSTOMINDREG_ENGA b010: bit 2 of register selected by CUSTOMINDREG_ENGA b011: bit 3 of register selected by CUSTOMINDREG_ENGA b100: bit 4 of register selected by CUSTOMINDREG_ENGA b101: bit 5 of register selected by CUSTOMINDREG_ENGA b110: bit 6 of register selected by CUSTOMINDREG_ENGA b111: bit 7 of register selected by CUSTOMINDREG_ENGA
		CUSTOMOUT_ENGA	15:0	RW	h0000	Defines the output value of the CustomStat engine A: Bit 0: Output value when [A,B,C,D]=[b0,b0,b0,b0] Bit 1: Output value when [A,B,C,D]=[b0,b0,b0,b1] Bit 2: Output value when [A,B,C,D]=[b0,b0,b1,b0] Bit 3: Output value when [A,B,C,D]=[b0,b0,b1,b1] Bit 4: Output value when [A,B,C,D]=[b0,b1,b0,b0] Bit 5: Output value when [A,B,C,D]=[b0,b1,b0,b1] Bit 6: Output value when [A,B,C,D]=[b0,b1,b1,b0] Bit 7: Output value when [A,B,C,D]=[b0,b1,b1,b1] Bit 8: Output value when [A,B,C,D]=[b1,b0,b0,b0] Bit 9: Output value when [A,B,C,D]=[b1,b0,b0,b1] Bit 10: Output value when [A,B,C,D]=[b1,b0,b1,b0] Bit 11: Output value when [A,B,C,D]=[b1,b0,b1,b1] Bit 12: Output value when [A,B,C,D]=[b1,b1,b0,b0] Bit 13: Output value when [A,B,C,D]=[b1,b1,b0,b1] Bit 14: Output value when [A,B,C,D]=[b1,b1,b1,b0] Bit 15: Output value when [A,B,C,D]=[b1,b1,b1,b1] For example if one wants CUSTOMSTATA=b1 as soon as C=b1, one must set CUSTOMOUT_ENGA=hCCCCCCCC.
8014	RegIrqCfg2	Reserved	31:30		b00	
		CUSTOMPINSEL_ENGA	29:24	RW	b000000	Maps CUSTOMSTATA to the corresponding pin: [29:24]=[NIRQ, CSIO4, CSIO3, CSIO2, CSIO1, CSIO0] This parameter is only valid if the corresponding pin is set as digital output (see RegPinCfg) Same pin should not be assigned to both CUSTOMSTATA and CUSTOMSTATB.
		Reserved	23:22		b00	
		CUSTOMPINSEL_ENGB	21:16	RW	b000000	Same as CUSTOMPINSEL_ENGA for engine B.
		CUSTOMINAREG_ENGB	15:12	RW	b0000	Same as CUSTOMINAREG_ENGA for engine B.
		Reserved	11		b0	
		CUSTOMINABIT_ENGB	10:8	RW	b000	Same as CUSTOMINABIT_ENGA for engine B.
		CUSTOMINBREG_ENGB	7:4	RW	b0000	Same as CUSTOMINBREG_ENGA for engine B.
		Reserved	3		b0	
		CUSTOMINBBIT_ENGB	2:0	RW	b000	Same as CUSTOMINBBIT_ENGA for engine B.
8018	RegIrqCfg3	CUSTOMINCREG_ENGB	31:28	RW	b0000	Same as CUSTOMINCREG_ENGA for engine B.
		Reserved	27		b0	
		CUSTOMINCBIT_ENGB	26:24	RW	b000	Same as CUSTOMINCBIT_ENGA for engine B.
		CUSTOMINDREG_ENGB	23:20	RW	b0000	Same as CUSTOMINDREG_ENGA for engine B.
		Reserved	19		b0	
		CUSTOMINDBIT_ENGB	18:16	RW	b000	Same as CUSTOMINDBIT_ENGA for engine B.
		CUSTOMOUT_ENGB	15:0	RW	h0000	Same as CUSTOMOUT_ENGA for engine B.

801C	RegScanPeriod	SCANFACTOR_PH0	31:30	RW	b00	Defines the scan period factor for phase 0: b00: 1x SCANPERIOD b01: 4x SCANPERIOD b10: 8x SCANPERIOD b11: 16x SCANPERIOD
		SCANFACTOR_PH1	29:28	RW	b00	Same as SCANFACTOR_PH0 for phase 1.
		SCANFACTOR_PH2	27:26	RW	b00	Same as SCANFACTOR_PH0 for phase 2.
		SCANFACTOR_PH3	25:24	RW	b00	Same as SCANFACTOR_PH0 for phase 3.
		SCANFACTOR_PH4	23:22	RW	b00	Same as SCANFACTOR_PH0 for phase 4.
		SCANFACTOR_PH5	21:20	RW	b00	Same as SCANFACTOR_PH0 for phase 5.
		Reserved	19:11		h000	
		SCANPERIOD	10:0	RW	h32	Defines the Active scan period: h00: Reserved Else: SCANPERIOD*(8192/FOsc) Default value is ~102 ms. Cf. FOsc/FTrim/FTemp/FVDD in electrical specifications. Note that SCANPERIOD should always be set higher than total sensing+processing time (i.e. CONVSTAT duration).
8020	RegGnrlCtrl2	Reserved	31:22		h000	
		COMPEN	21:16	RW	b000000	Defines the phases to compensate when the host sends compensation command: b0: Off b1: On [21:16] = [PH5, PH4, PH3, PH2, PH1, PH0]
		Reserved	15:10		b000000	
		DOZEPERIOD	9:8	RW	b00	Enables Doze mode and defines its scan period: b00: Off b01: 4x SCANPERIOD b10: 8x SCANPERIOD b11: 16x SCANPERIOD Note that this setting applies to all phases and doze period will automatically clamp to ~4s max.
		Reserved	7:6		b00	
		PHEN	5:0	RW	b000000	Enables sensing/measurement phases: b0: Off b1: On [5:0] = [PH5, PH4, PH3, PH2, PH1, PH0] When any PHEN bit is set a compensation is automatically performed for that phase. When PHEN set to b000000, wait for 1 Scan Period minimum (i.e. Sensing time configured) to allow device change to occur. Note that changing PHEN from b000000 to any other value will not start sensing until the proper command is sent (see RegCmd).
8024	RegAfeParamsPh0	Reserved	31:30		b00	
		RINT_PH0	29:28	RW	b11	Defines the internal compensation resistor for phase 0: b00: $R_{INTUNIT}$ (~125Ω) b01: $R_{INTUNIT}$ *2 (~250Ω) b10: $R_{INTUNIT}$ *8 (~1kΩ) b11: $R_{INTUNIT}$ *16 (~2kΩ) Cf. $R_{INTUNIT}$ in electrical specifications.
		RESFILTIN_PH0	27:24	RW	b0000	Defines the pre-charge input resistor for phase 0: b0000: 0/Off b0001: $R_{FILTINUNIT}$ (~2 kΩ) b0010: $R_{FILTINUNIT}$ *2 (~4 kΩ) b0011: $R_{FILTINUNIT}$ *3 (~6 kΩ) b0100: $R_{FILTINUNIT}$ *4 (~8 kΩ) b0101: $R_{FILTINUNIT}$ *5 (~10 kΩ)

						b0110: RFILTINUNIT *6 (~12 kΩ) b0111: RFILTINUNIT *7 (~14 kΩ) b1000: RFILTINUNIT *8 (~16 kΩ) b1001: RFILTINUNIT *9 (~18 kΩ) b1010: RFILTINUNIT *10 (~20 kΩ) b1011: RFILTINUNIT *11 (~22 kΩ) b1100: RFILTINUNIT *12 (~24 kΩ) b1101: RFILTINUNIT *13 (~26 kΩ) b1110: RFILTINUNIT *14 (~28 kΩ) b1111: RFILTINUNIT *15 (~30 kΩ) Cf. RFILTINUNIT in electrical specifications.
		Reserved	23:13		h000	
		AGAIN_PH0	12:9	RW	b0010	Defines the analog range for phase 0: b0000: Reserved b0001: CRANGEUNIT *2 (+/- ~1.1 pF) b0010: CRANGEUNIT *3 (+/- ~1.65 pF) b0011: CRANGEUNIT *4 (+/- ~2.2 pF) b0100: CRANGEUNIT *6 (+/- ~3.3 pF) b0101: CRANGEUNIT *7 (+/- ~3.85 pF) b0110: CRANGEUNIT *8 (+/- ~4.4 pF) b0111: CRANGEUNIT *9 (+/- ~4.95 pF) b1000: CRANGEUNIT *10 (+/- ~5.5 pF) b1001: CRANGEUNIT *11 (+/- ~6.05 pF) b1010: CRANGEUNIT *12 (+/- ~6.6 pF) b1011: CRANGEUNIT *13 (+/- ~7.15 pF) b1100: CRANGEUNIT *15 (+/- ~8.25 pF) b1101: CRANGEUNIT *16 (+/- ~8.8 pF) b1110: CRANGEUNIT *17 (+/- ~9.35 pF) b1111: CRANGEUNIT *18 (+/- ~9.9 pF) Cf. CRANGEUNIT in electrical specifications.
		Reserved	8		b0	
		FREQ_PH0	7:3	RW	b11010	Defines the sampling frequency for phase 0: b00000: FOsc/16 (~250 kHz) b00001: FOsc/20 (~200 kHz) b00010: FOsc/24 (~166.67 kHz) b00011: FOsc/28 (~142.86 kHz) b00100: FOsc/32 (~125 kHz) b00101: FOsc/36 (~111.11 kHz) b00110: FOsc/40 (~100 kHz) b00111: FOsc/44 (~90.91 kHz) b01000: FOsc/48 (~83.33 kHz) b01001: FOsc/52 (~76.92 kHz) b01010: FOsc/56 (~71.43 kHz) b01011: FOsc/60 (~66.67 kHz) b01100: FOsc/64 (~62.50 kHz) b01101: FOsc/68 (~58.82 kHz) b01110: FOsc/72 (~55.56 kHz) b01111: FOsc/76 (~52.63 kHz) b10000: FOsc/80 (~50 kHz) b10001: FOsc/88 (~45.45 kHz) b10010: FOsc/96 (~41.67 kHz) b10011: FOsc/104 (~38.46 kHz) b10100: FOsc/112 (~35.71 kHz) b10101: FOsc/128 (~31.25 kHz) b10110: FOsc/144 (~27.78 kHz) b10111: FOsc/ 160 (~25 kHz) b11000: FOsc/ 192 (~20.83 kHz) b11001: FOsc/224 (~17.86 kHz) b11010: FOsc/288 (~13.89 kHz) b11011: FOsc/352 (~11.36 kHz) b11100: FOsc/480 (~8.33 kHz) b11101: FOsc/608 (~6.58 kHz)

						b11110: FOsc/ 736 (~5.43 kHz) b11111: FOsc/ 864 (~4.63 kHz) Cf. FOsc/FTrim/FTemp/FVDD in electrical specifications.
		RESOLUTION_PH0	2:0	RW	b100	Defines the measurement precision for phase 0: b000: 8 b001: 16 b010: 32 b011: 64 b100: 128 b101: 256 b110: 512 b111: 1024
8028	RegAfePhPh0	AFEMEASSELECT_PH0	31:30	RW	b00	Defines the measurement performed during phase 0: b00: Capacitance (see AFEPHCSx_PH0) b01: Voltage b10: Temperature b11: Reserved
		AFEPHCS4_PH0	29:27	RW	b000	Defines the usage of CSIO4 during phase 0: b000: Given by register RegPinCfg When AFEMEASSELECT_PH0=b00 (Capacitance): b100: HZ b101: Measured Input b110: Dynamic Shield b111: GND When AFEMEASSELECT_PH0=b01 (Voltage): b100: HZ b101: Measured Input Else: Reserved When AFEMEASSELECT_PH0=b10 (Temperature): b100: HZ Else: Reserved
		AFEPHCS3_PH0	26:24	RW	b000	Same as AFEPHCS4_PH0 for CSIO3.
		AFEPHCS2_PH0	23:21	RW	b000	Same as AFEPHCS4_PH0 for CSIO2.
		AFEPHCS1_PH0	20:18	RW	b000	Same as AFEPHCS4_PH0 for CSIO1.
		AFEPHCS0_PH0	17:15	RW	b000	Same as AFEPHCS4_PH0 for CSIO0.
		PROXOFFSET_PH0	14:0	RW	h0000	Current value of compensation offset for phase 0. Unsigned.
802C	RegAfeParamsPh1	Same as RegAfeParamsPh0 for phase 1.				
8030	RegAfePhPh1	Same as RegAfePhPh0 for phase 1.				
8034	RegAfeParamsPh2	Same as RegAfeParamsPh0 for phase 2.				
8038	RegAfePhPh2	Same as RegAfePhPh0 for phase 2.				
803C	RegAfeParamsPh3	Same as RegAfeParamsPh0 for phase 3.				
8040	RegAfePhPh3	Same as RegAfePhPh0 for phase 3.				
8044	RegAfeParamsPh4	Same as RegAfeParamsPh0 for phase 4.				
8048	RegAfePhPh4	Same as RegAfePhPh0 for phase 4.				
804C	RegAfeParamsPh5	Same as RegAfeParamsPh0 for phase 5.				
8050	RegAfePhPh5	Same as RegAfePhPh0 for phase 5.				
Digital Processing Control						
8054	RegAdcFiltPh0	Reserved	31:29		b000	
		ADCFILTCOEFIN_PH0	28:27	RW	b00	Defines the in-range coefficient of the ADC filter for phase 0: b00: 0 b01: 1/4 b10: 1/2 b11: 1
		DIFFTHRESHFACT_PH0	26:24	RW	b000	Defines the multiplication factor applied to PROX/BODY/TABLETHRESH and

						STEADYMAXVAR for phase 0: b000: x1 (Off) b001: x2 b010: x4 b011: x8 b100: x16 b101: x32 b110: x64 b111: Reserved
		Reserved	23		b0	
		RAWFILTCOEF_PH0	22:20	RW	b001	Defines the strength of the RAW filter for phase 0: b000: 0 (Off) b001: 1-1/2 b010: 1-1/4 b011: 1-1/8 b100: 1-1/16 b101: 1-1/32 b110: 1-1/64 b111: 1-1/128
		ADCFILTSAMPLES_PH0	19:18	RW	b00	Defines the number of samples of the ADC filter for phase 0: b00: 1 (Off) b01: 2 b10: 4 b11: 8
		ADCFILTCOEFOUT_PH0	17:16	RW	b00	Defines the out-of-range coefficient of the ADC filter for phase 0: b00: 1 b01: 1/2 b10: 1/4 b11: 1/8
		PROXTHRESH_PH0	15:8	RW	h00	Defines the proximity threshold for phase 0: h00: 0 h01: 1 Else: int[PROXTHRESH_PH0^2/2] Note that DIFFTHRESHFACT_PH0 applies.
		Reserved	7		b0	
		FARCOND_PH0	6	RW	b0	Defines far/release/non-prox condition for phase 0: b0 : PROXDIFF < (THRESH-HYST) b1 : PROXDIFF < - (THRESH-HYST) FARCOND_PH0=b1 is typically used with AVGFREEZEDIS_PH0=b1.
		HYST_PH0	5:4	RW	b00	Defines the proximity detection hysteresis applied to PROX/BODY/TABLETHRESH_PH0: b00: None b01: Small b10: Medium b11: High Small/Medium/High values correspond to a binary right shift of the threshold by respectively 4/3/2 bits, hence approximately +/- 6/12/25%.
		CLOSEDEB_PH0	3:2	RW	b00	Defines the Close debouncer applied to PROX/BODY/TABLETHRESH_PH0: b00: Off b01: 2 samples b10: 4 samples b11: 8 samples
		FARDEB_PH0	1:0	RW	b00	Defines the Far debouncer applied to PROX/BODY/TABLETHRESH_PH0: b00: Off b01: 2 samples

						b10: 4 samples b11: 8 samples
8058	RegAvgBFiltPh0	AVGTHRESHINIT_PH0	31	RW	b0	Defines the initial value used to calculate average thresholds for phase 0: b0: 0 b1: Average value after last compensation
		AVGCOMPMETH_PH0	30	RW	b0	Defines the average compensation method for phase 0: b0: Individual, phase 0 triggers only its own compensation. b1: Common, phase 0 triggers compensation of all enabled phases
		AVGNEGTHRESH_PH0	29:24	RW	b100000	Defines the negative average threshold that will trigger compensation for phase 0: AVGTHRESHINIT_PH0 – (16384*AVGNEGTHRESH_PH0) Default value (if AVGTHRESHINIT_PH0=b0) is -524288. Typically set between +/-524288 and +/-786432 (i.e. ½ to ¾ of the system dynamic range). Compensation will be triggered for phase 0 only or for all enabled phases, depending on AVGCOMPMETHOD_PH0.
		AVGDEB_PH0	23:22	RW	b01	Defines the average debouncer applied to AVGPOS/AVGNEGTHRESH_PH0: b00: Off b01: 2 samples b10: 4 samples b11: 8 samples
		AVGPOSTHRESH_PH0	21:16	RW	b100000	Defines the positive average threshold which will trigger compensation for phase 0: b000000: OFF, no automatic compensation; both from positive and negative thresholds. Else: AVGTHRESHINIT_PH0 + (16384*AVGPOSTHRESH_PH0) Default value (if AVGTHRESHINIT_PH0=b0) is 524288. Typically set between 524288 and 786432 (i.e. ½ to ¾ of the system dynamic range). When AVGTHRESHINIT_PH0=b0, should not be set below b010000 except to turn it OFF by setting it to b000000. When AVGTHRESHINIT_PH0=b1, should not be set above b110000. Compensation will be triggered for phase 0 only or for all enabled phases, depending on AVGCOMPMETHOD_PH0.
		Reserved	15		b0	
		AVGFREEZEDIS_PH0	14	RW	b0	Disables Average freezing during prox for phase 0: b0: On, as soon as prox is detected, average is frozen until prox is released. b1: Off, as soon as prox is detected, average is frozen for 4*AVGDEB_PH0 samples and then unfrozen (even if prox is not released). This setting is only applicable when the USE filter is disabled.
		AVGNEGFILT_PH0	13:11	RW	b001	Defines the strength of the AVG negative filter for phase 0: b000: 0 (Off) b001: 1-1/2 b010: 1-1/4 b011: 1-1/8

						b100: 1-1/16 b101: 1-1/32 b110: 1-1/64 b111: 1 (Infinite)
		AVGPOSFILT_PH0	10:8	RW	b100	Defines the strength of the AVG positive filter for phase 0: b000: 0 (Off) b001: 1-1/32 b010: 1-1/64 b011: 1-1/128 b100: 1-1/256 b101: 1-1/512 b110: 1-1/1024 b111: 1 (Infinite)
		USETHRSHNODET_PH0	7:0	RW	h00	Defines the non-detection threshold of the USE filter for phase 0: h00: 0 h01: 0.0625 h02: 0.125 … hFF: 15.9375 Coded on 8bits unsigned as XXXX.YYYY.
805C	RegAvgAFiltPh0	USETHRSHDETPOS_PH0	31:24	RW	h00	Defines the positive detection threshold of the USE filter for phase 0: h00: 0 h01: 0.0625 … h7F: 7.9375 h80: -8 h81: -7.9375 … hFF: -0.0625 Coded on 8bits signed (2's complement) as XXXX.YYYY.
		USETHRSHDETNEG_PH0	23:16	RW	h00	Defines the negative detection threshold of the USE filter for phase 0: h00: 0 h01: 0.0625 … h7F: 7.9375 h80: -8 h81: -7.9375 … hFF: -0.0625 Coded on 8bits signed (2's complement) as XXXX.YYYY.
		USEFILTFACT_PH0	15:13	RW	b000	Defines the multiplication factor applied to all 6 USE filter thresholds and correction values for phase 0: b000: x1 b001: x2 b010: x4 b011: x8 b100: x16 b101: x32 b110: x64 b111: x128
		USEFILTENABLE_PH0	12	RW	b0	Enables the USE filter for phase 0: b0: Off b1: On
		USECORRNODET_PH0	11:8	RW	b0000	Defines the non-detection correction value of the USE filter for phase 0:

						b0000: 0 … b0111: 7 b1000: -8 b1001: -7 … b1111: -1 Signed, 2's complement.
		USECORRDETPOS_PH0	7:4	RW	b0000	Defines the positive detection correction value of the USE filter for phase 0: b0000: 0 … b0111: 7 b1000: -8 b1001: -7 … b1111: -1 Signed, 2's complement.
		USECORRDETNEG_PH0	3:0	RW	b0000	Defines the negative detection correction value of the USE filter for phase 0: b0000: 0 … b0111: 7 b1000: -8 b1001: -7 … b1111: -1 Signed, 2's complement.
8060	RegAdvDig0Ph0	STARTUPFREQ_PH0	31	RW	b0	Defines when the start-up detection is performed for phase 0: b0: Only after PHEN compensation b1: After each compensation
		OFFSETTHRESH_PH0	30:16	RW	h0000	Enables start-up proximity detection and defines offset threshold for phase 0: h0000: Off, no start-up detection performed Else: Start-up detection offset threshold. After compensation is performed, PROXOFFSET_PH0 is temporarily forced to OFFSETTHRESH_PH0 and PROXUSEFUL_PH0 compared to USEFULTHRESH_PH0 (PROXAVG_PH0 and PROXDIFF_PH0 frozen) If [PROXUSEFUL_PH0>USEFULTHRESH_PH0] => Set PROXSTAT_PH0 to b1, and set it back to b0 only when [[PROXUSEFUL_PH0<USEFULTHRESH_PH0], then run compensation and start normal processing. Else => Set PROXSTAT_PH0 to b0, restore original PROXOFFSET and start normal processing.
		USEFULTHRESH_PH0	15:0	RW	h0000	Defines the useful threshold for start-up detection for phase 0: 32*USEFULTHRESH_PH0 Signed, 2's complement.
8064	RegAdvDig1Ph0	Reserved	31:24		h00	
		BODYTHRESH_PH0	23:16	RW	h00	Defines the body threshold for phase 0: h00: Off h01: 1 Else: int[BODYTHRESH_PH0^2/2] Note that DIFFTHRESHFACT_PH0 applies.
		TABLETHRESHHIGH_PH0	15:8	RW	h00	Defines the high table threshold for phase 0:

						h00: Off (both high and low thresholds) h01: 1 Else: int[TABLETHRESHHIGH_PH0^2/2] Note that DIFFTHRESHFACT_PH0 applies.
		TABLETHRESHLOW_PH0	7:0	RW	h00	Defines the low table threshold for phase 0: h00: 0 h01: 1 Else: int[TABLETHRESHLOW_PH0^2/2] Note that DIFFTHRESHFACT_PH0 applies.
8068	RegAdvDig2Ph0	Reserved	31:30		b00	
		STEADYEN_PH0	29:28	RW	b00	Enables the steady detection for phase 0, and defines to which signal it applies: b00: Off b01: PROXDIFF_PH0, only when PROXSTAT_PH0=b1 b10: PROXDIFF_PH0, all the time b11: PROXUSEFUL_PH0, all the time
		STEADYWINDOW_PH0	27:26	RW	b00	Defines the length of the steady window during which peak-peak variation is checked against STEADYMAXVAR_PH0: b00: 4 samples b01: 16 samples b10: 64 samples b11: 128 samples
		UNSTEADYDEB_PH0	25:24	RW	b00	Defines the number of consecutive and unsuccessful STEADYWINDOW_PH0s required to clear STEADYSTAT_PH0: b00: Off b01: 2 b10: 4 b11: 8
		Reserved	23		b0	
		STEADYCOND_PH0	22:20	RW	b000	Enables steady condition status flags for phase 0: [2:0]=[PROXSTAT_PH0, BODYSTAT_PH0, TABLESTAT_PH0] b0: Off b1: On, PROX/BODY/TABLE status flag is set only if the corresponding STEADYSTAT is set also (logic AND). Else: Reserved. Bit2/MSB should not be set if STEADYEN_PH0=b01.
		STEADYMAXVAR_PH0	19:16	RW	b0000	Defines the maximum tolerated peak-peak variation (LSBs) during each STEADYWINDOW_PH0: b0000: 0 b0001: 1 b0010: 2 b0011: 4 b0100: 8 b0101: 16 b0110: 32 b0111: 64 b1000: 128 b1001: 256 b1010: 512 b1011: 1024 b1100: 2048 b1101: 4096 b1110: 8192 b1111: 16384 Note that DIFFTHRESHFACT_PH0 applies.

		Reserved	15:12		b0000	
		STEADYDEB_PH0	11:8	RW	b0000	Defines the number of consecutive and successful STEADYWINDOW_PH0s required to set STEADYSTAT_PH0: b0000: 1 b0001: 2 b0010: 3 b0011: 7 b0100: 11 b0101: 15 b0110: 23 b0111: 31 b1000: 39 b1001: 55 b1010: 71 b1011: 87 b1100: 119 b1101: 151 b1110: 183 b1111: 247
		Reserved	7:6		b00	
		SATDEB_PH0	5:4	RW	b00	Defines the debouncer applied to set the saturation detection flag for phase 0: b00: Off b01: 2 samples b10: 4 samples b11: 8 samples
		SATCANCELEN_PH0	3:2	RW	b00	Enables saturation detection/compensation for phase 0: b00: Off b10: Detection only b11: Detection and compensation Else: Reserved
		SATTHRESH_PH0	1:0	RW	b00	Defines the saturation threshold for phase 0: b00: 640000 b01: 768000 b10: 896000 b11: 1024000
806C	RegAdvDig3Ph0	REFCOEFINCA_PH0	31:24	RW	h00	Defines the increase coefficient of engine A for phase 0: h00: 0 h01: 0.03125 h02: 0.0625 … h20: 1 … hFF: 7.96875 Coded on 8 bits as XXX.YYYYY.
		REFCOEFINCB_PH0	23:16	RW	h00	Same as REFCOEFINCA_PH0 for engine B.
		REFCOEFDECA_PH0	15:8	RW	h00	Defines the decrease coefficient of engine A for phase 0: h00: 0 h01: 0.03125 h02: 0.0625 … h20: 1 … hFF: 7.96875 Coded on 8 bits as XXX.YYYYY.
		REFCOEFDECB_PH0	7:0	RW	h00	Same as REFCOEFDECA_PH0 for engine B.
8070	RegAdvDig4Ph0	Reserved	31:22		h000	
		REFCOEFSIGN_PH0	21:18	RW	b0000	Defines the signs of the coefficients for phase 0:

						[21:18]=[REFCOEFDECB_PH0, REFCOEFDECA_PH0, REFCOEFINCB_PH0, REFCOEFINCA_PH0] b0: + b1: -
		REFCORRENABLE_PH0	17:16	RW	b00	Enables and defines which reference correction engines apply to phase 0: b00: None/Off, phase 0 is not corrected b01: Engine A only b10: Engine B only b11: Engine A and Engine B
		FAILTHRESHHIGH_PH0	15:8	RW	h00	Enables and defines the high threshold of failure detection for phase 0: h00: Off (high threshold only) hFF: Saturation (32767 or 0) Else: 128*FAILTHRESHHIGH_PH0 Note that failure check is only performed after compensation or after PROXOFFSET_PH0 is forced by I2C (i.e. not when FAILTHRESHHIGH_PH0 value is modified).
		FAILTHRESHLOW_PH0	7:0	RW	h00	Enables and defines the low threshold of failure detection for phase 0: h00: Off (low threshold only) Else: 128*FAILTHRESHLOW_PH0 Note that failure check is only performed after compensation or after PROXOFFSET_PH0 is forced by I2C (i.e. not when FAILTHRESHLOW_PH0 value is modified).
8074	RegAdcFiltPh1	Same as RegAdcFiltPh0 for phase 1.				
8078	RegAvgBFiltPh1	Same as RegAvgBFiltPh0 for phase 1.				
807C	RegAvgAFiltPh1	Same as RegAvgAFiltPh0 for phase 1.				
8080	RegAdvDig0Ph1	Same as RegAdvDig0Ph0 for phase 1.				
8084	RegAdvDig1Ph1	Same as RegAdvDig1Ph0 for phase 1.				
8088	RegAdvDig2Ph1	Same as RegAdvDig2Ph0 for phase 1.				
808C	RegAdvDig3Ph1	Same as RegAdvDig3Ph0 for phase 1.				
8090	RegAdvDig4Ph1	Same as RegAdvDig4Ph0 for phase 1.				
8094	RegAdcFiltPh2	Same as RegAdcFiltPh0 for phase 2.				
8098	RegAvgBFiltPh2	Same as RegAvgBFiltPh0 for phase 2.				
809C	RegAvgAFiltPh2	Same as RegAvgAFiltPh0 for phase 2.				
80A0	RegAdvDig0Ph2	Same as RegAdvDig0Ph0 for phase 2.				
80A4	RegAdvDig1Ph2	Same as RegAdvDig1Ph0 for phase 2.				
80A8	RegAdvDig2Ph2	Same as RegAdvDig2Ph0 for phase 2.				
80AC	RegAdvDig3Ph2	Same as RegAdvDig3Ph0 for phase 2.				
80B0	RegAdvDig4Ph2	Same as RegAdvDig4Ph0 for phase 2.				
80B4	RegAdcFiltPh3	Same as RegAdcFiltPh0 for phase 3.				
80B8	RegAvgBFiltPh3	Same as RegAvgBFiltPh0 for phase 3.				
80BC	RegAvgAFiltPh3	Same as RegAvgAFiltPh0 for phase 3.				
80C0	RegAdvDig0Ph3	Same as RegAdvDig0Ph0 for phase 3.				
80C4	RegAdvDig1Ph3	Same as RegAdvDig1Ph0 for phase 3.				
80C8	RegAdvDig2Ph3	Same as RegAdvDig2Ph0 for phase 3.				
80CC	RegAdvDig3Ph3	Same as RegAdvDig3Ph0 for phase 3.				
80D0	RegAdvDig4Ph3	Same as RegAdvDig4Ph0 for phase 3.				
80D4	RegAdcFiltPh4	Same as RegAdcFiltPh0 for phase 4.				
80D8	RegAvgBFiltPh4	Same as RegAvgBFiltPh0 for phase 4.				
80DC	RegAvgAFiltPh4	Same as RegAvgAFiltPh0 for phase 4.				
80E0	RegAdvDig0Ph4	Same as RegAdvDig0Ph0 for phase 4.				
80E4	RegAdvDig1Ph4	Same as RegAdvDig1Ph0 for phase 4.				
80E8	RegAdvDig2Ph4	Same as RegAdvDig2Ph0 for phase 4.				
80EC	RegAdvDig3Ph4	Same as RegAdvDig3Ph0 for phase 4.				
80F0	RegAdvDig4Ph4	Same as RegAdvDig4Ph0 for phase 4.				
80F4	RegAdcFiltPh5	Same as RegAdcFiltPh0 for phase 5.				

80F8	RegAvgBFiltPh5	Same as RegAvgBFiltPh0 for phase 5.				
80FC	RegAvgAFiltPh5	Same as RegAvgAFiltPh0 for phase 5.				
8100	RegAdvDig0Ph5	Same as RegAdvDig0Ph0 for phase 5.				
8104	RegAdvDig1Ph5	Same as RegAdvDig1Ph0 for phase 5.				
8108	RegAdvDig2Ph5	Same as RegAdvDig2Ph0 for phase 5.				
810C	RegAdvDig3Ph5	Same as RegAdvDig3Ph0 for phase 5.				
8110	RegAdvDig4Ph5	Same as RegAdvDig4Ph0 for phase 5.				
Step Cancellation Engines						
8114	RegStepCancel0A	STEPNOSATCOND_ENGA	31	RW	b0	Enables saturation condition for step correction engine A: b0: Off, step can always be corrected b1: On, step can be corrected only if saturation is not detected for the phase selected by STEPCANCELPH_ENGA
		STEPCANCELEN_ENGA	30:29	RW	b00	Enables step detection/correction engine A: b00: Off b10: Detection only b11: Detection and correction Else: Reserved When enabled, the step detection works only under the following conditions: - STEPCANCELXA_ENGA, STEPCANCELXB_ENGA and STEPCANCELXC_ENGA are not equal to 0 - (STEPCANCELXA_ENGA + STEPCANCELXB_ENGA + STEPCANCELXC_ENGA) ≤ 12
		STEPCANCELPH_ENGA	28:26	RW	b000	Defines to which phase step cancellation engine A applies: b000: PH0 b001: PH1 b010: PH2 b011: PH3 b100: PH4 b101: PH5 Else: Reserved
		STEPCANCELXB_ENGA	25:23	RW	b000	Defines the number of samples during which the signal must change significantly, for engine A: b000: 0 b001: 1 … b111: 7
		STEPCANCELXC_ENGA	22:19	RW	b0000	Defines the number of samples during which the signal must be stable after a step, for engine A: b0000: 0 b0001: 1 … b1111: 15
		STEPCANCELXA_ENGA	18:15	RW	b0000	Defines the number of samples during which the signal must be stable prior to a step, for engine A: b0000: 0 b0001: 1 … b1111: 15
		STEPCANCELYB_ENGA	14:0	RW	h0000	Defines the min variation during XB for engine A: 32*STEPCANCELYB_ENGA
8118	RegStepCancel1A	Reserved	31:27		b00000	
		STEPCANCELYA_ENGA	26:16	RW	h000	Defines the max variation during XA for engine A: 8*STEPCANCELYA_ENGA
		Reserved	15:11		b00000	
		STEPCANCELYC_ENGA	10:0	RW	h000	Defines the max variation during XC for engine A: 8*STEPCANCELYC_ENGA

811C	RegStepCancel0B	Same as RegStepCancel0A for engine B.				
8120	RegStepCancel1B	Same as RegStepCancel1A for engine B.				
Reference Correction Engines						
8124	RegRefCorrA	Reserved	31:27		b00000	
		REFENABLE_ENGA	26	RW	b0	Enables reference correction engine A: b0: Off b1: On, engine A is applied when selected (see REFCORRENABLE_PHx)
		REFCAL_ENGA	25:4	RW	h000000	Defines the reference calibration value for engine A (Cf. REFINIT_ENGA) Signed, 2's complement format.
		REFINIT_ENGA	3	RW	b0	Defines how RefUseful0C (first reference value after compensation) is initialized (power-up or other) for engine A: b0: REFCAL_ENGA b1: PROXUSEFUL of REFPHASE_ENGA
		REFPHASE_ENGA	2:0	RW	b000	Defines which phase is used as reference for engine A: b000: PH0 b001: PH1 b010: PH2 b011: PH3 b100: PH4 b101: PH5 Else: Reserved
8128	RegRefCorrB	Same as RegRefCorrA for engine B.				
Smart SAR Engines						
812C	RegSmartSar0A	Reserved	31:13		h0000	
		SMARTSAREN_ENGA	12	RW	b0	Enables the smart SAR engine A: b0: Off b1: On
		SMARTSARDEB_ENGA	11:10	RW	b00	Defines the debouncer applied to the SAR threshold for engine A: b00: Off b01: 2 samples b10: 4 samples b11: 8 samples
		SMARTSARHYST_ENGA	9:8	RW	b00	Defines the hysteresis applied to the SAR threshold for engine A: b00: None b01: Small b10: Medium b11: High Small/Medium/High values correspond to a binary right shift of the threshold by respectively 4/3/2 bits, hence approximately +/- 6/12/25%.
		Reserved	7:6		b00	
		SMARTSAREXTPH_ENGA	5:3	RW	b000	Defines the external phase of the smart SAR engine A: b000: PH0 b001: PH1 b010: PH2 b011: PH3 b100: PH4 b101: PH5 Else: Reserved The selected phase must be enabled in PHEN.
		SMARTSARINTPH_ENGA	2:0	RW	b000	Defines the internal phase of the smart SAR engine A: b000: PH0 b001: PH1 b010: PH2

						b011: PH3 b100: PH4 b101: PH5 Else: Reserved The selected phase must be enabled in PHEN.
8130	RegSmartSar1A	SMARTSARX0_ENGA	31:15	RW	h0000	Defines the Point0 abscissa of the smart SAR threshold for engine A. Unsigned 17bits.
		SMARTSARDELTAX23_ENGA	14:10	RW	b00000	Defines the delta between Point2 and Point3 abscissas of the smart SAR threshold for engine A. b00000: 2^0 (1) b00001: 2^1 (2) … b10011: 2^19 (524288) Else: Reserved SMARTSARX3=SMARTSARX0 + SMARTSARDELTAX01 + SMARTSARDELTAX12 + SMARTSARDELTAX23
		SMARTSARDELTAX12_ENGA	9:5	RW	b00000	Defines the delta between Point1 and Point2 abscissas of the smart SAR threshold for engine A. b00000: 2^0 (1) b00001: 2^1 (2) … b10011: 2^19 (524288) Else: Reserved SMARTSARX2=SMARTSARX0 + SMARTSARDELTAX01 + SMARTSARDELTAX12
		SMARTSARDELTAX01_ENGA	4:0	RW	b00000	Defines the delta between Point0 and Point1 abscissas of the smart SAR threshold for engine A. b00000: 2^0 (1) b00001: 2^1 (2) … b10011: 2^19 (524288) Else: Reserved SMARTSARX1=SMARTSARX0 + SMARTSARDELTAX01
8134	RegSmartSar2A	SMARTSARY0_ENGA	31:15	RW	h0000	Defines the Point0 ordinate of the smart SAR threshold for engine A. Unsigned 17bits.
		SMARTSARDELTAY23_ENGA	14:10	RW	b00000	Defines the delta between Point2 and Point3 ordinates of the smart SAR threshold for engine A. b00000: 2^0 (1) b00001: 2^1 (2) … b10011: 2^19 (524288) Else: Reserved SMARTSARY3=SMARTSARY0 + SMARTSARDELTAY01 + SMARTSARDELTAY12 + SMARTSARDELTAY23
		SMARTSARDELTAY12_ENGA	9:5	RW	b00000	Defines the delta between Point1 and Point2 ordinates of the smart SAR threshold for engine A. b00000: 2^0 (1) b00001: 2^1 (2) … b10011: 2^19 (524288) Else: Reserved SMARTSARY2=SMARTSARY0 + SMARTSARDELTAY01 + SMARTSARDELTAY12
		SMARTSARDELTAY01_ENGA	4:0	RW	b00000	Defines the delta between Point0 and Point1 ordinates of the smart SAR threshold for engine A. b00000: 2^0 (1)

						b00001: 2^1 (2) … b10011: 2^19 (524288) Else: Reserved SMARTSARY1=SMARTSARY0 + SMARTSARDELTAY01
8138	RegSmartSar0B	Same as RegSmartSar0A for engine B.				
813C	RegSmartSar1B	Same as RegSmartSar1A for engine B.				
8140	RegSmartSar2B	Same as RegSmartSar2A for engine B.				
8144	RegSmartSar0C	Same as RegSmartSar0A for engine C.				
8148	RegSmartSar1C	Same as RegSmartSar1A for engine C.				
814C	RegSmartSar2C	Same as RegSmartSar2A for engine C.				
Prox2Pwm Engine						
8150	RegProx2PwmA	PROX2PWMINIT	31	RW	b0	Defines the reference level of the PROX2PWM engine: b0: First value after last compensation b1: PROX2PWMOFF
		PROX2PWMINPUT	30	RW	b0	Defines the input signal of the PROX2PWM engine: b0: PROXUSEFUL b1: PROXDIFF
		PROX2PWMPOL	29	RW	b0	Defines the mapping polarity of the PROX2PWM engine: b0: negative (PWMLEVELA decreases when input signal increases) b1: positive (PWMLEVELA increases when input signal increases)
		PROX2PWMOFF	28:9	RW	h00000	Defines the offset of the PROX2PWM engine. Coded as signed, 2's complement.
		PROX2PWMFUNC	8	RW	b0	Defines the transfer function of the PROX2PWM engine: b0: Proportional, PWMLEVELA = PROX2PWMGAIN*(PROX2PWMINPUT - 2*PROX2PWMOFF) b1: Integral, PWMLEVELA = PWMLEVELA + PROX2PWMGAIN*(PROX2PWMINPUT - 2*PROX2PWMOFF).
		PROX2PWMEN	7	RW	b0	Enables the PROX2PWM engine: b0: Off b1: On, PWMLEVELA is updated by PROX2PWM engine
		PROX2PWMGAIN	6:3	RW	b0000	Defines the gain of the PROX2PWM engine: b0000: 1 b0001: 1 / 2 b0010: 1 / 4 b0011: 1 / 8 b0100: 1 / 16 b0101: 1 / 32 b0110: 1 / 64 b0111: 1 / 128 b1000: 1 / 256 b1001: 1 / 512 b1010: 1 / 1024 b1011: 1 / 2048 b1100: 1 / 4096 b1101: 1 / 8192 b1110: 1 / 16384 b1111: 1 / 32768
		PROX2PWMPHASE	2:0	RW	b000	Defines which phase is used by the PROX2PWM engine: b000: PH0 b001: PH1

						b010: PH2 b011: PH3 b100: PH4 b101: PH5 Else: Reserved
Auto Sampling Frequency						
8154	RegAutoFreq0	AUTOFREQMASK	31:0	RW	h00000000	Enables the frequencies to be used by the automatic sampling frequency feature: b0: Off b1: On [31:0]=[FREQ_PHx(b11111), …, FREQ_PHx(b00000)] For example, to select only FREQ_PHx(b11111) and FREQ_PHx(b00000), one must set AUTOFREQMASK to h80000001.
8158	RegAutoFreq1	Reserved	31:28	RW	h0	
		AUTOFREQENABLE_PH5	27:26	RW	b00	Enables the automatic sampling frequency feature for phase 5: b00: Off b01: Only after PHEN compensation b10: After both PHEN and manual/I2C compensation b11: After any compensation, except those triggered by automatic sampling frequency feature itself
		AUTOFREQENABLE_PH4	25:24	RW	b00	Same as AUTOFREQENABLE_PH5 for phase 4.
		AUTOFREQENABLE_PH3	23:22	RW	b00	Same as AUTOFREQENABLE_PH5 for phase 3.
		AUTOFREQENABLE_PH2	21:20	RW	b00	Same as AUTOFREQENABLE_PH5 for phase 2.
		AUTOFREQENABLE_PH1	19:18	RW	b00	Same as AUTOFREQENABLE_PH5 for phase 1.
		AUTOFREQENABLE_PH0	17:16	RW	b00	Same as AUTOFREQENABLE_PH5 for phase 0.
		Reserved	15:4		h000	
		AUTOFREQCOMP	3	RW	b0	Enables compensation during frequency sweep: b0: Off b1: On, compensation is forced after each frequency setting, before measuring noise level
		AUTOFREQSAMPLES	2:0	RW	b000	Defines the number of PROXADC samples used by the automatic sampling frequency feature to measure noise level: b000: 2 b001: 4 b010: 8 b011: 16 b100: 32 b101: 64 b110: 128 b111: 256
Main Data Readback						
815C	RegUsePh0	PROXUSEFUL_PH0	31:0	RW	h00000000	Current Useful value of phase 0. Coded as signed, 2's complement: [31:0] = XXXXXXXXXXXXXXXXXXXXX.YYYYYYYYYY
8160	RegUsePh1	Same as RegUsePh0 for phase 1.				
8164	RegUsePh2	Same as RegUsePh0 for phase 2.				
8168	RegUsePh3	Same as RegUsePh0 for phase 3.				
816C	RegUsePh4	Same as RegUsePh0 for phase 4.				
8170	RegUsePh5	Same as RegUsePh0 for phase 5.				
8174	RegAvgPh0	PROXAVG_PH0	31:0	RW	h00000000	Current Average value of phase 0. Coded as signed, 2's complement: [31:0] = XXXXXXXXXXXXXXXXXXXXX.YYYYYYYYYY
8178	RegAvgPh1	Same as RegAvgPh0 for phase 1.				
817C	RegAvgPh2	Same as RegAvgPh0 for phase 2.				

8180	RegAvgPh3	Same as RegAvgPh0 for phase 3.				
8184	RegAvgPh4	Same as RegAvgPh0 for phase 4.				
8188	RegAvgPh5	Same as RegAvgPh0 for phase 5.				
818C	RegDiffPh0	PROXDIFF_PH0	31:0	RW	h00000000	Current Diff value of phase 0. Coded as signed, 2's complement: [31:0] = XXXXXXXXXXXXXXXXXXXXX.YYYYYYYYYY
8190	RegDiffPh1	Same as RegDiffPh0 for phase 1.				
8194	RegDiffPh2	Same as RegDiffPh0 for phase 2.				
8198	RegDiffPh3	Same as RegDiffPh0 for phase 3.				
819C	RegDiffPh4	Same as RegDiffPh0 for phase 4.				
81A0	RegDiffPh5	Same as RegDiffPh0 for phase 5.				
Debug Data Readback						
81A4	RegDbgVarSel	Reserved	31:16		h01F0	
		Reserved	15:6		h000	
		PHASESEL	5:3	RW	b000	Defines the phase of debug variables available in registers RegDgbVar0/1/2/3/4: b000: PH0 b001: PH1 b010: PH2 b011: PH3 b100: PH4 b101: PH5 Else: Reserved
		Reserved	2		b0	
		ENGINESEL	1:0	RW	b00	Define the engine of debug variables available in registers RegDbgVar5/6/7/8: b00: Engine A b01: Engine B b10: Engine C (smart SAR only) b11: Reserved
81A8	RegDbgVar0	ADCFILTMIN_PHx	31:0	RW	h00000000	Current min value of the PROXADC of the phase selected by PHASESEL (ADC filter). Coded as signed, 2's complement: [31:0] = XXXXXXXXXXXXXXXXXXXXX.YYYYYYYYYY
81AC	RegDbgVar1	ADCFILTMAX_PHx	31:0	RW	h00000000	Current max value of the PROXADC of the phase selected by PHASESEL (ADC filter). Coded as signed, 2's complement: [31:0] = XXXXXXXXXXXXXXXXXXXXX.YYYYYYYYYY
81B0	RegDbgVar2	RAWBEFORECORR_PHx	31:0	RW	h00000000	Current PROXRAW value before correction of the phase selected by PHASESEL (reference correction). Coded as signed, 2's complement: [31:0] = XXXXXXXXXXXXXXXXXXXXX.YYYYYYYYYY
81B4	RegDbgVar3	USEFILTDELTAVAR_PHx	31:0	RW	h00000000	Current variation value of the phase selected by PHASESEL (USE filter). Coded as signed, 2's complement: [31:0] = XXXXXXXXXXXXXXXXXXXXXXXXXXX.YYYY
81B8	RegDbgVar4	STEADYPEAKPEAK_PHx	31:0	RW	h00000000	Current peak-to-peak value of the phase selected by PHASESEL (steady detection). Coded as signed, 2's complement: [31:0] = XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
81BC	RegDbgVar5	STEPCANCELSUMA_ENGx	31:0	RW	h00000000	Current variation during XA of the engine selected by ENGINESEL (step cancellation). Coded as signed, 2's complement: [31:0] = XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

81C0	RegDbgVar6	STEPCANCELSUMB_ENGx	31:0	RW	h00000000	Current variation during XB of the engine selected by ENGINESEL (step cancellation). Coded as signed, 2's complement: [31:0] = XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
81C4	RegDbgVar7	STEPCANCSUMC_ENGx	31:0	RW	h00000000	Current variation during XC of the engine selected by ENGINESEL (step cancellation). Coded as signed, 2's complement: [31:0] = XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
81C8	RegDbgVar8	SMARTSARTHRESH_ENGx	31:0	RW	h00000000	Current threshold of the engine selected by ENGINESEL (smart SAR). Coded as signed, 2's complement: [31:0] = XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

Table 9: Registers Detailed Description

8. Application Information

8.1. Typical Application Circuit

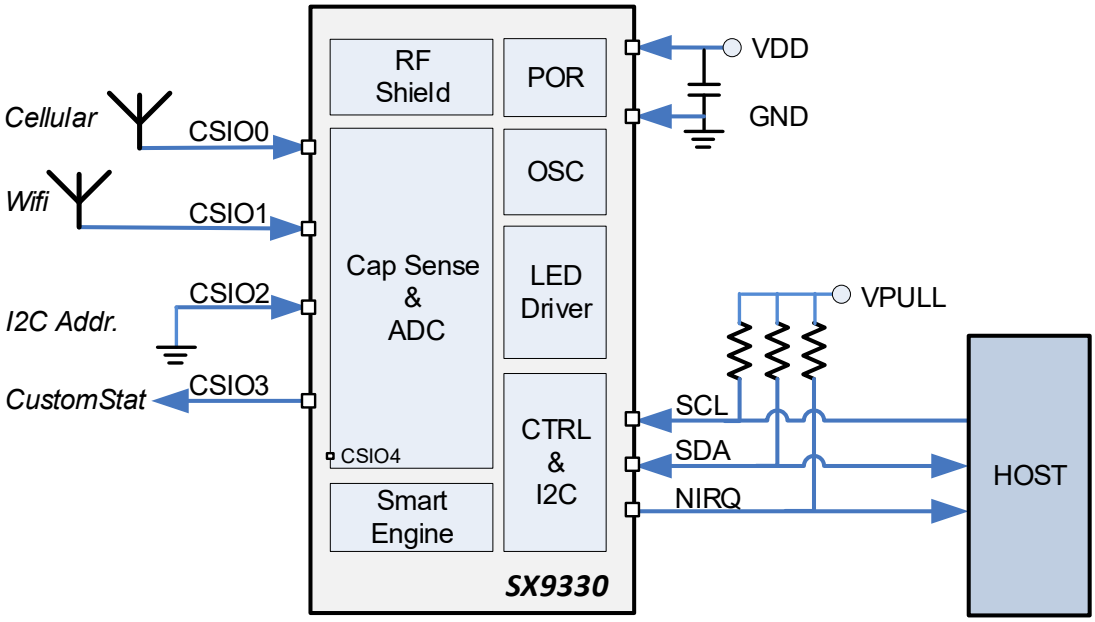


Figure 25: Typical Application Circuit

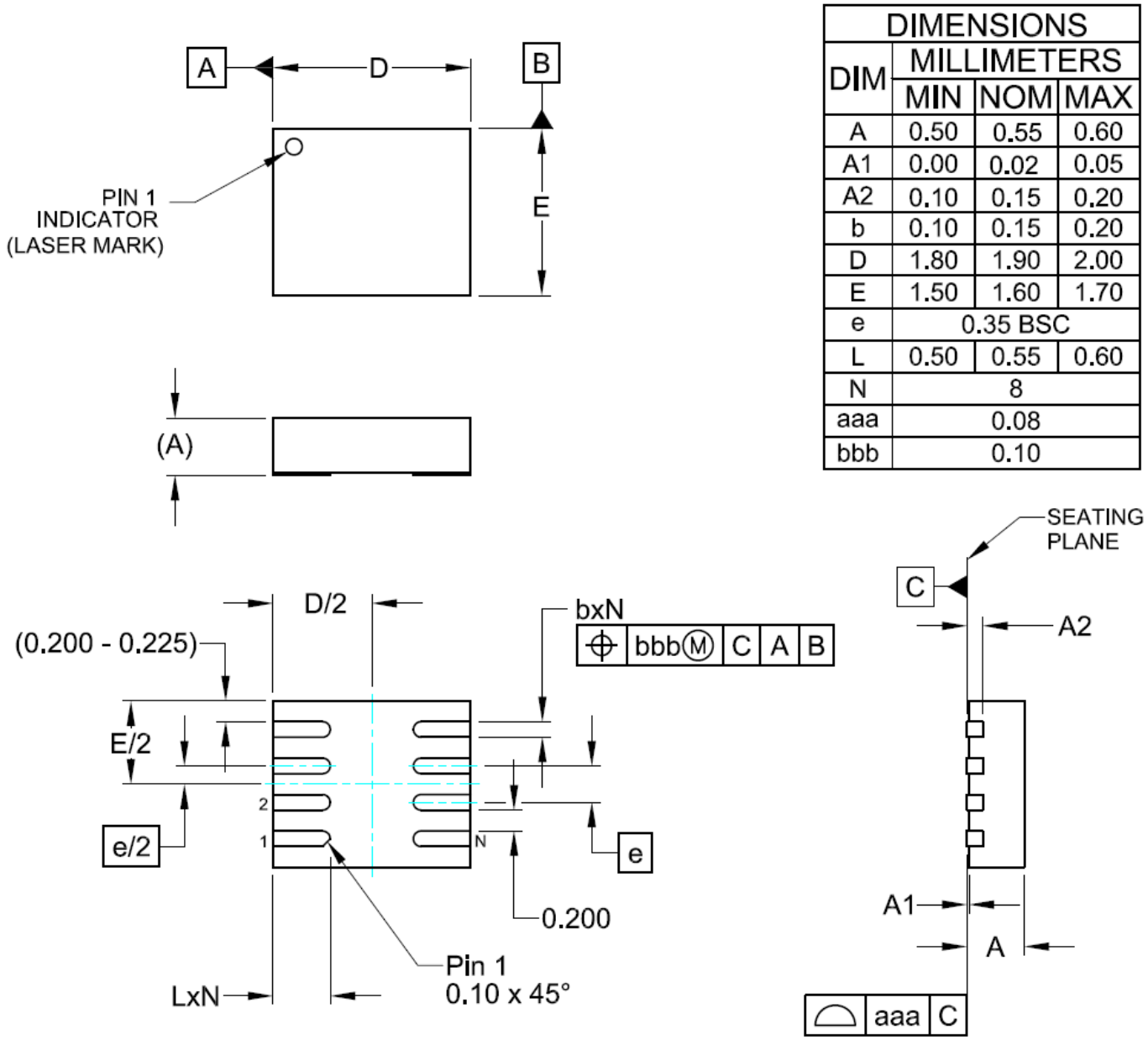
8.2. External Components Recommended Values

Symbol	Description	Note	Min	Typ.	Max	Unit
CDD	Supply Decoupling Capacitor	min X5R type, min 6.3V rating.	0.8	1	1.2	uF
RPULL	Host Interface Pull-ups		-	2.2	-	kΩ

Table 10: External Components Recommended Values

9. Packaging Information

9.1. Outline Drawing



DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A2	0.10	0.15	0.20
b	0.10	0.15	0.20
D	1.80	1.90	2.00
E	1.50	1.60	1.70
e	0.35 BSC		
L	0.50	0.55	0.60
N	8		
aaa	0.08		
bbb	0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

Figure 26: Outline Drawing – DFN Package

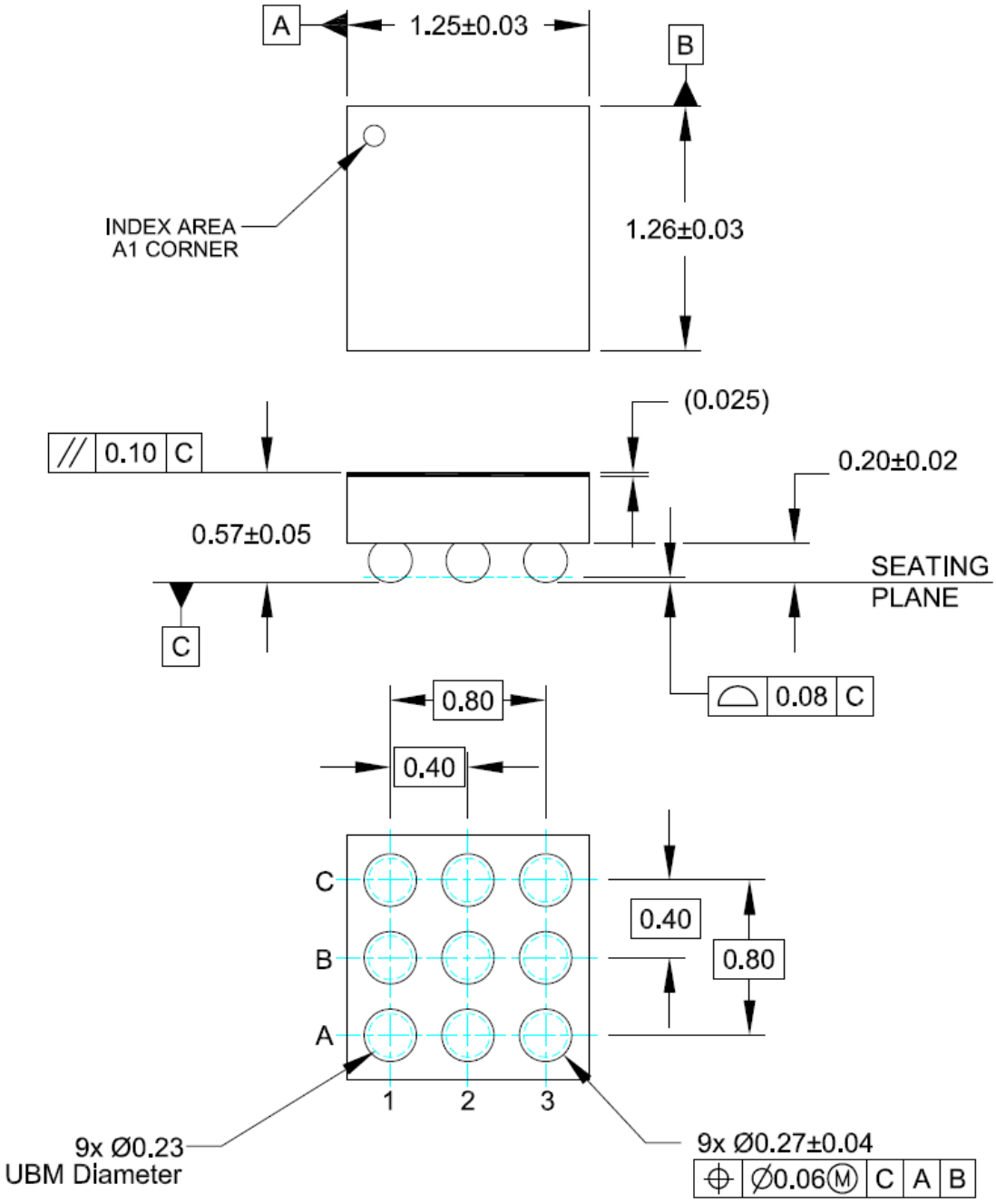
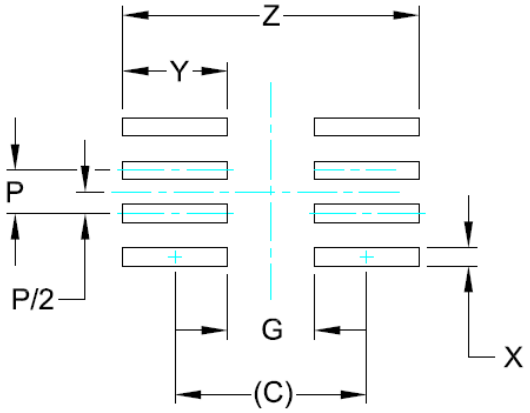


Figure 27: Outline Drawing – WLCSP Package

9.2. Land Pattern

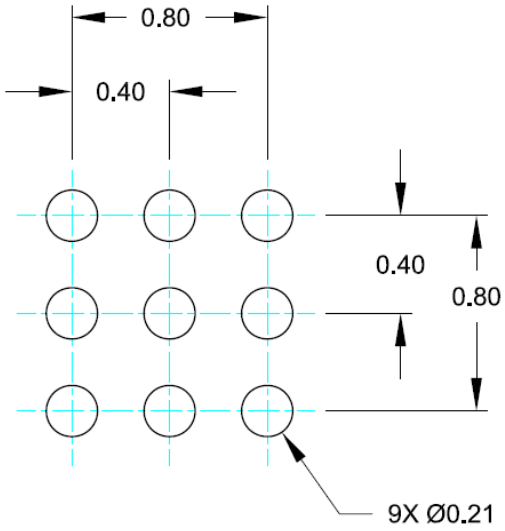


DIMENSIONS	
DIM	MILLIMETERS
C	(1.55)
G	0.70
P	0.35
X	0.15
Y	0.85
Z	2.40

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Figure 28: Land Pattern – DFN Package



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Figure 29: Land Pattern – WLCSP Package

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