RAPIDRF-26E39 OVERVIEW

2496-2690 MHz, 38.5 dBm, 27 V RF FRONT-END DESIGN

ORDERABLE PART NUMBER: RAPIDRF-26E39

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CONTENTS

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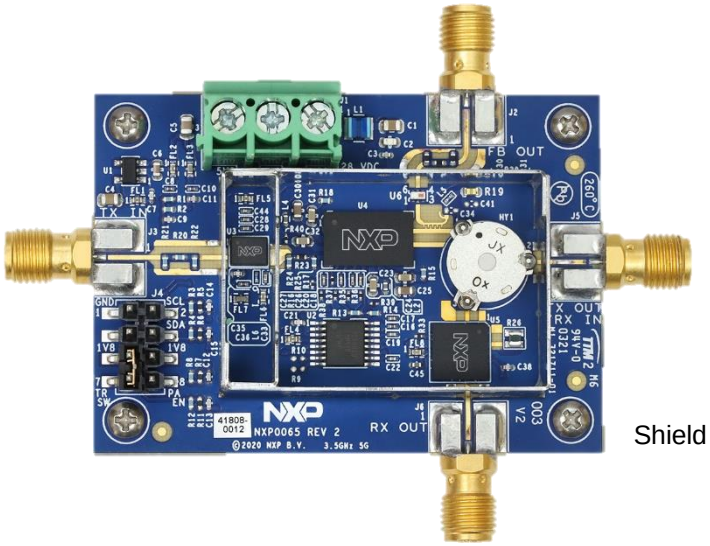
INTRODUCTION

- NXP’s RapidRF front-end designs are complete RF front-end solutions for 5G TDD radio systems. They are ideal for transmitters requiring 2.5 to 5 watts (34-37 dBm) average at the antenna with approximately 8.5 dB PAR LTE/NR signals.

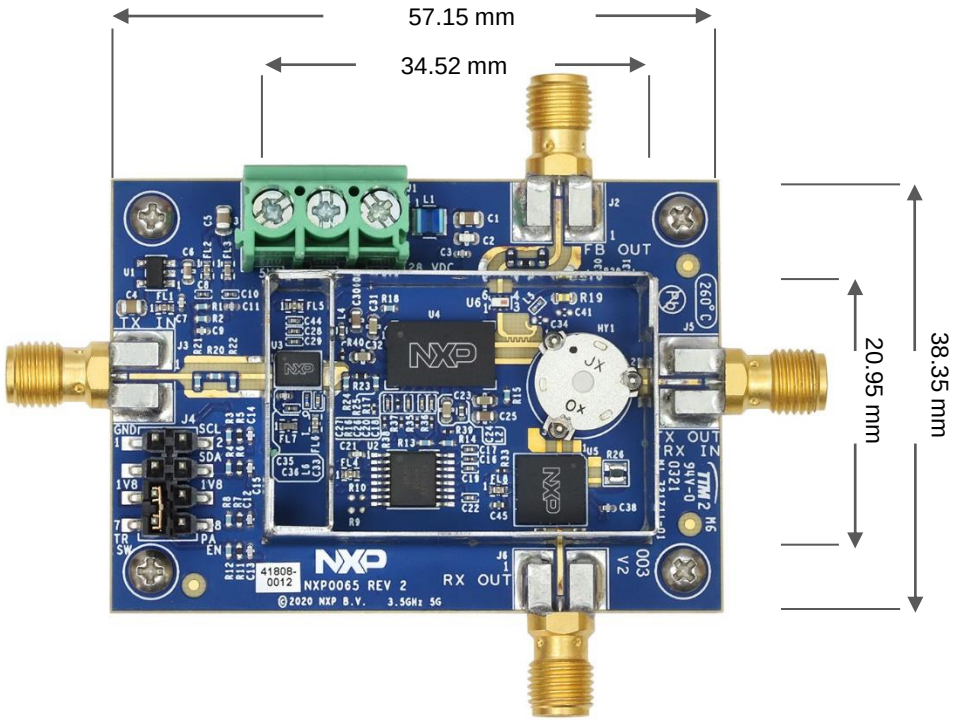
- The designs feature high efficiency Doherty power amplifier Multi-Chip Modules (PAMs) and can be linearized up to 200 MHz instantaneous bandwidth while meeting regulatory emissions requirements when used in conjunction with digital pre-distortion.

- The RapidRF series uses a common PCB layout, simplifying both design and manufacturing.



Shield cover removed

CIRCUIT OVERVIEW – 5.7 cm × 3.8 cm (2.25″ × 1.5″)



Top of cover to the PCB is 10.5 mm

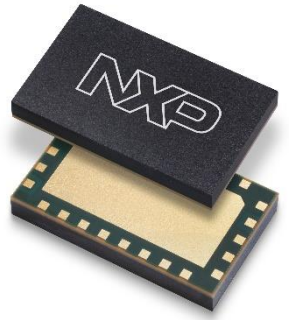
RAPIDRF SERIES FEATURES AND TARGET APPLICATIONS

Features

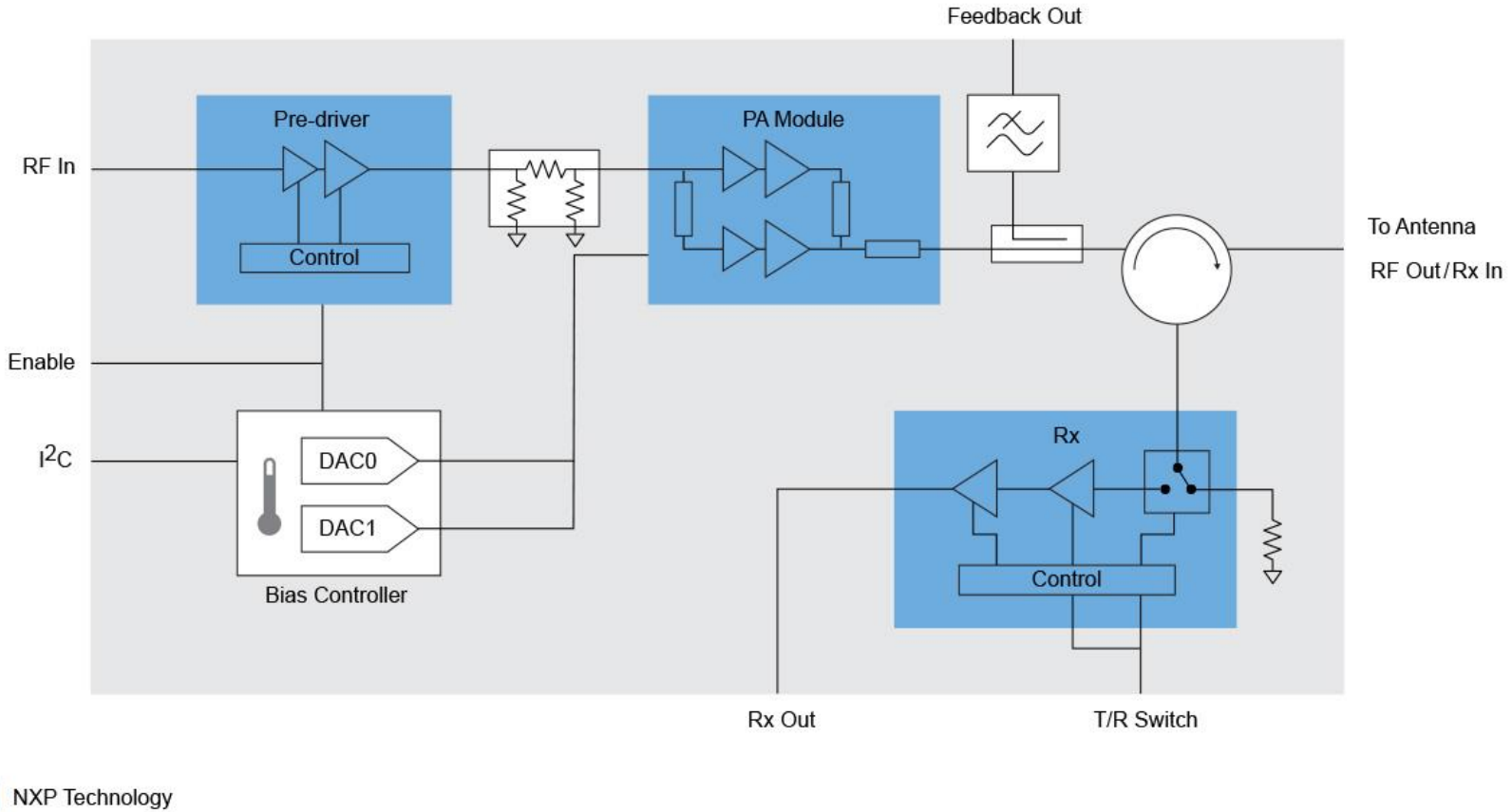
- Meets regulatory emissions requirements with capable DPD system
- Up to 200 MHz instantaneous bandwidth
- Up to 8 W average power
- Enhanced Doherty efficiency
- Integrated switch
- Pre-programmed bias controller with temperature compensation
- Circulator included
- Compact footprint
- Pre-distortion system feedback port

Target Applications

- 5G massive MIMO radio units (32T32R, 64T64R)
- Outdoor small cells
- Drivers for traditional macro base stations
- Open RAN and proprietary radio access networks



BLOCK DIAGRAM

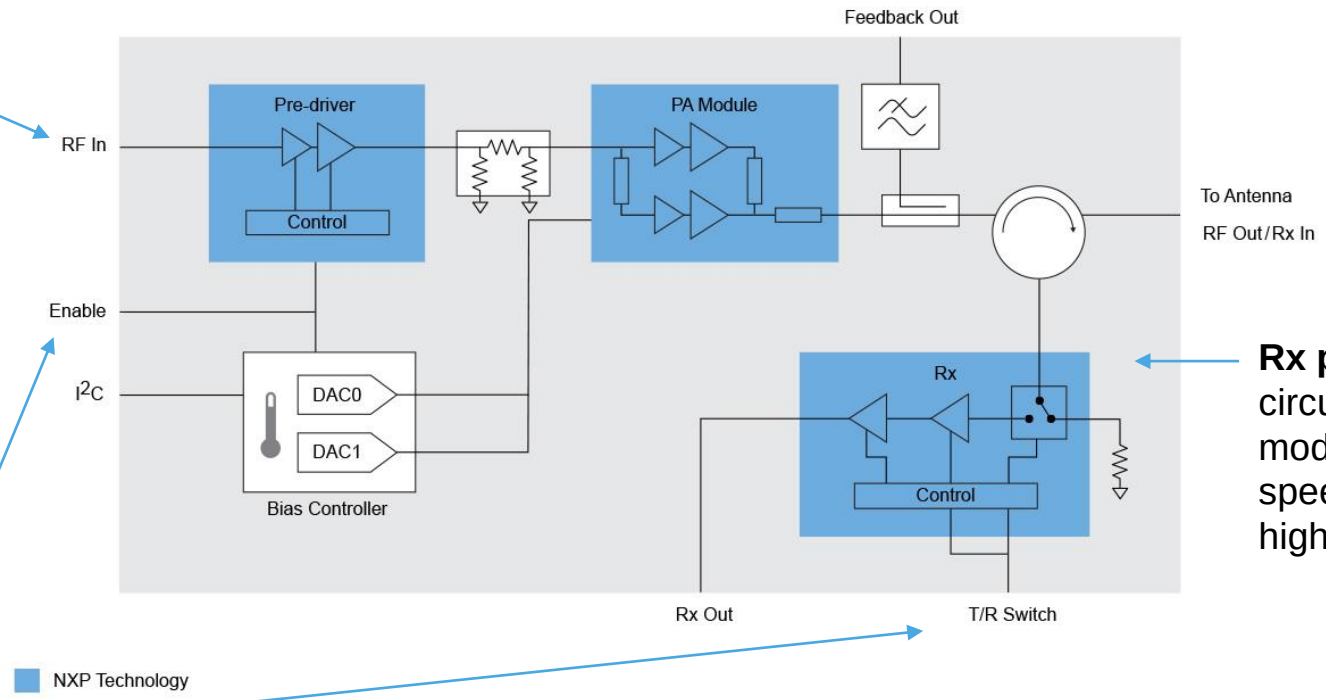


NXP Technology

SYSTEM DESCRIPTION

Tx output coupling is provided for wideband RF feedback required for digital pre-distortion (DPD).

Tx path: the RapidRF designs integrate a pre-driver multi-chip module driving a Doherty RF power multi-chip module connected through a circulator to the antenna port. The Tx path amplifies low-level signals (≤-10 dBm) from the RF modulator output up to full antenna output power.



Rx path: the antenna port and circulator feed into the Rx LNA module which includes a high-speed switch ahead of a low noise, high intercept point amplifier.

TDD control is enabled by logic levels on 2 pins, one to enable the power amplifier and the other to enable the receive sub-system and control switch. Bias settings are factory pre-programmed.

MAIN COMPONENTS

Pre-driver

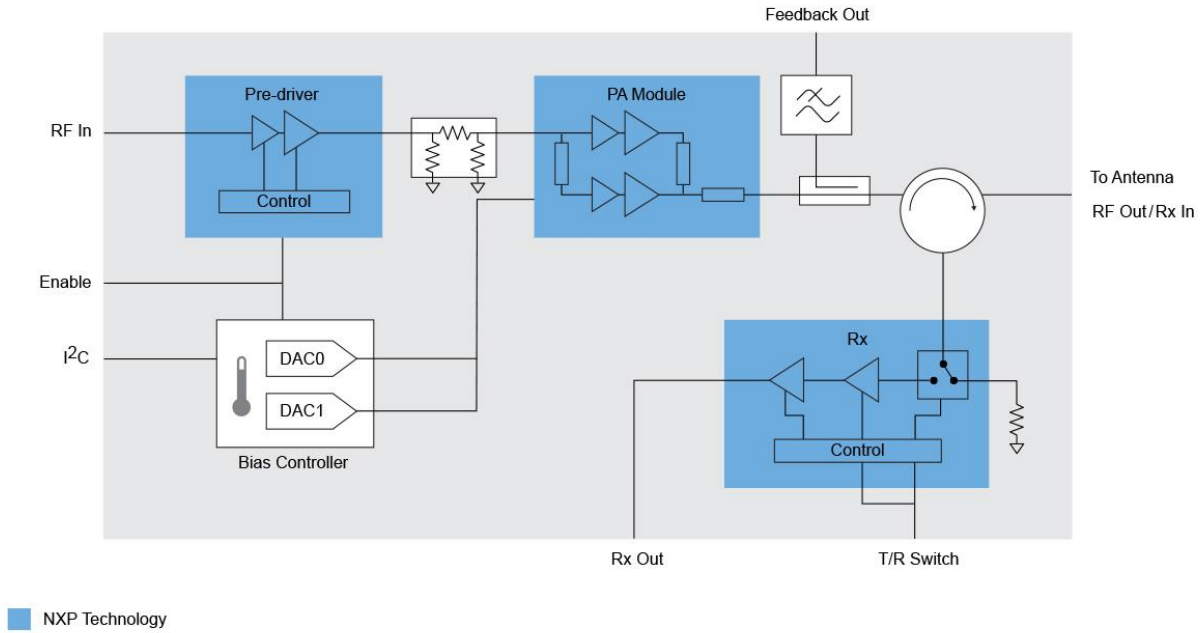
High linearity GaAs pre-driver amplifier, with fast on-off switching to support TDD systems.

AFLP5G25641 data sheet

Bias Controller

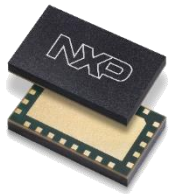
Pre-programmed monitor/controller measures temperature and sets optimum bias points for amplifier stages inside the PAM.

TI LMP92066 data sheet



Power Amplifier Multi-Chip Module (PAM)

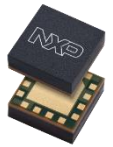
2-stage LDMOS Doherty amplifier with integrated matching.



AFSC5G26E39 data sheet

Rx / Switch Devices

Analog front-end receive module with high-speed switch and GaAs low noise amplifiers.



AFRX5G272 data sheet

TECHNICAL DETAILS

Tx Pre-driver Multi-Chip Module

- The power levels into the pre-driver module are designed for approximately -20 dBm average with a typical PAR (peak-to-average ratio) of approximately 10 dB. The output power is approximately 13 dBm average. The pre-driver is operated in class A or AB linear to simplify error correction. The signal is routed through a 2 dB attenuator that provides improved isolation and match to the integrated PAM.

PAM (Power Amplifier Multi-Chip Module)

- The PAM is a two-stage LDMOS Doherty amplifier. Both the input and output are matched to 50 ohms, simplifying layout and design complexity. Bias for each of the devices within the PAM are pinned out to enable precise control of the idle currents. The bias can be internally temperature compensated or, as in the case of the RapidRF modules, can be externally set and temperature compensated by the bias controller. The amplifier output is sampled by a 38 dB coupler before the circulator to provide a wideband DPD feedback signal. The through path from the coupler is connected to the antenna port through a circulator.

Receive Switch /LNA

- The receive pre-amplifier is connected to the antenna port through the circulator and switch. The switch protects the pre-amplifier from overload when transmitting. The preamplifier has a low noise figure with high intercept point and wide bandwidth.

Circulator

- The circulator provides both a stable impedance for the transmitter and low loss path to the receiver, minimizing noise. In transmit mode the circulator isolation port is connected through the switch to a termination. In receive mode the isolation port is connected through the switch to the LNA.

Bias Controller

- The controller is pre-programmed to provide optimal bias levels for all PAM stages. The controller integrated temperature sensor compensates the bias voltages according to pre-programmed values. The controller also provides low-impedance bias drive to optimize the switching speed needed for TDD systems.

TYPICAL PERFORMANCE – RAPIDRF-26E39

Tx Path

Typical Single-Carrier W-CDMA Performance: Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF, Uncorrected Configuration

Frequency (MHz)	Average Power (dBm)	Lineup Gain (dB)	Lineup Efficiency (%)	Output PAR (dB)	Output stage V_{DD} (V)
2496-2690	**38.5**	**55.9**	**37.4**	**8.5**	**27**

Rx Path

Frequency (MHz)	Gain (dB)	Noise Figure (dB)	IIP3 (dBm)	OIP3 (dBm)
2496-2690	**32**	**1.6**	**0**	**32**

Supply Requirements

Current Consumption (mA)			V_{DD} Output Stage Voltage
5 V Rx	5 V Tx	Tx Output 24-32 V	V_{DD}
105	**75**	**740**	**27**

The values shown are the average performance numbers across the frequency range.

Connectors

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J4 CONTROL CONNECTOR PINOUT

J4 Control Connector

Pin	Name	Function	Limits
1	Ground	Ground	
2	SCL	I²C clock for bias controller programming	1.8 V logic 2.0 V max. (Factory use only)
3	N.C.		
4	SDA	I²C data for bias controller programming	1.8 V logic 2.0 V max. (Factory use only)
5	1.8 V Internal		200 µA sink or source max combined.
6	1.8 V Internal		
7	Transmit /Receive Switch	0 = Receive mode. 1 = Transmit mode.	1.8 V logic 2.0 V max. Internal 180 µA pull down.
8	PA Enable	0 = PA standby. 1 = PA enable.	

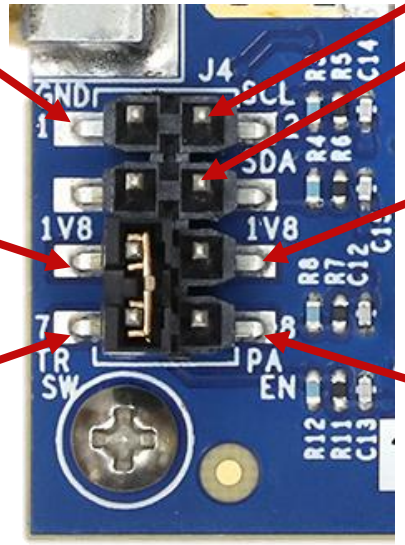
Ground

On-board 1.8 V Supply

- Can use a jumper to combine with T/R switch pin to fix EVB in Rx state

Transmit/Receive Switch

- 0 V defaults Rx switch to transmit mode and disables Rx LNA
- Apply 1.8 V to toggle Rx switch from transmit to receive mode and enable Rx LNA



I²C Serial Clock and Data

- 1.8 V Logic
- Can be used to access and program bias controller component (not required for operation)

On-board 1.8 V Supply

- Can use a jumper with PA Enable pin to fix Tx driver and final stage in enable state

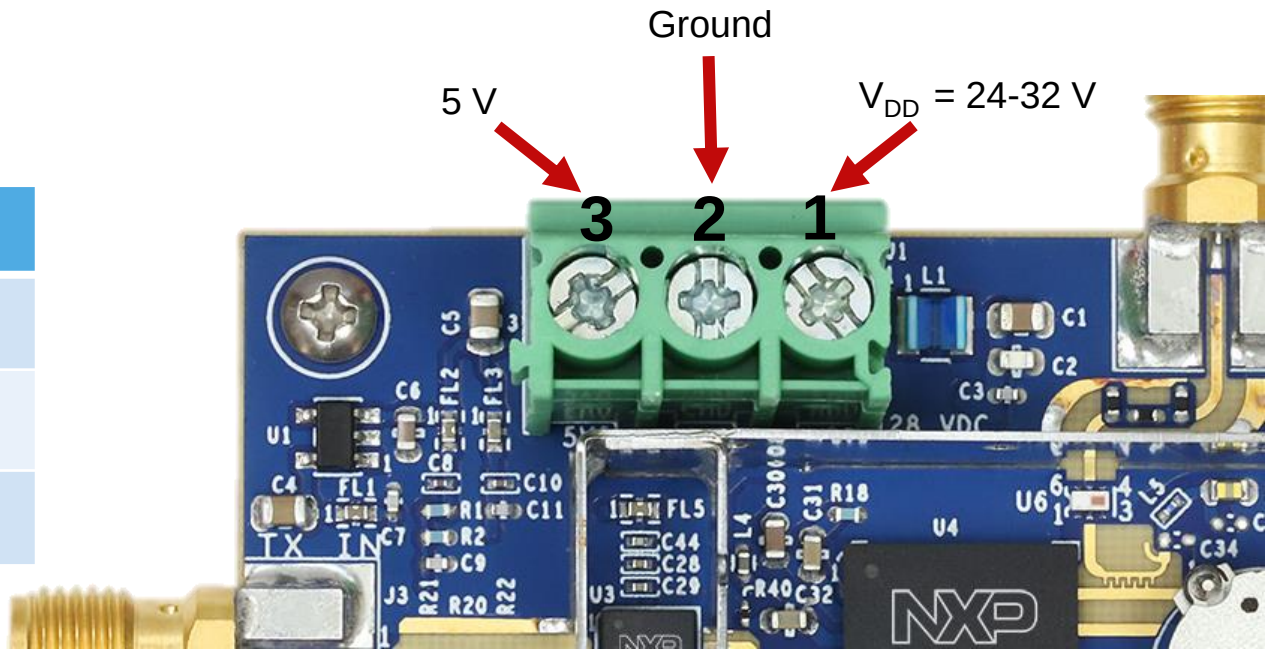
PA Enable

- Asserting PA Enable turns on both Tx devices
- Apply 1.8 V to enable Tx driver and final stage

J1 POWER CONNECTOR PINOUT

J1 Power Connector

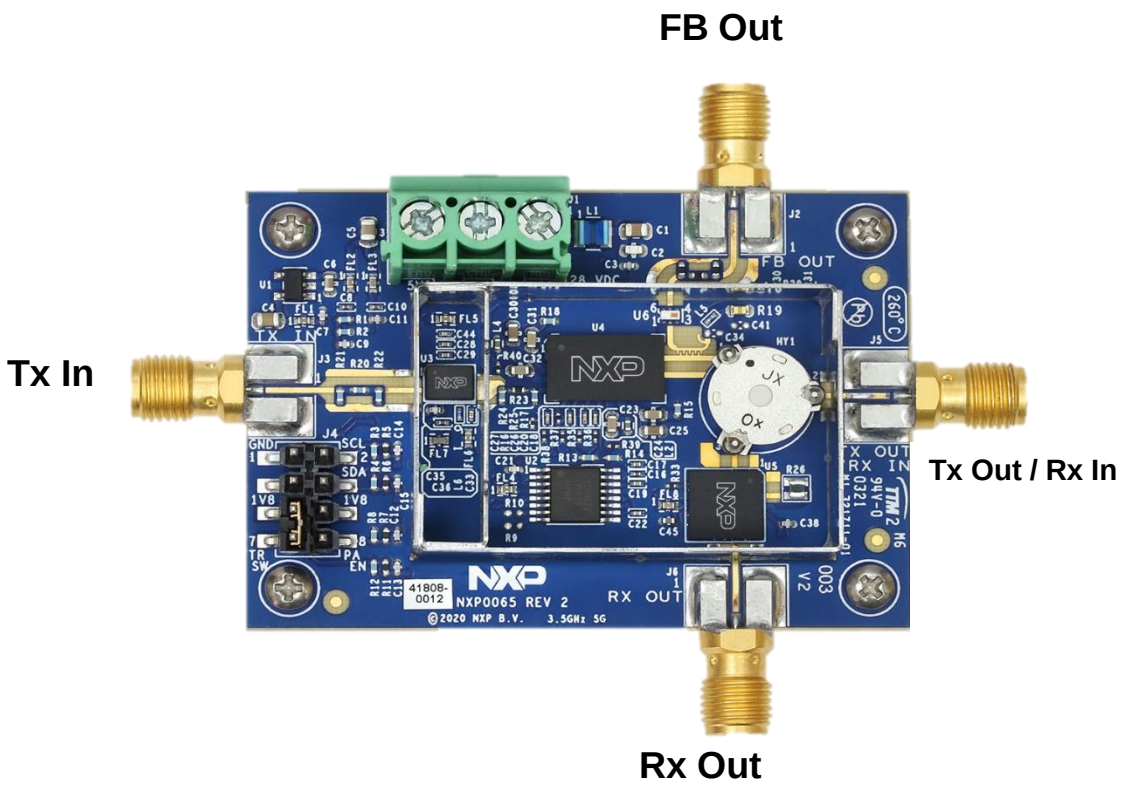
Pin	Name	Function	Limits
1	V_{DD}	PA supply	32 V max, 1000 mA max.
2	Ground	Ground	
3	5 V	Supply for logic, receive and pre-driver	5.25 V max, 150 mA max.



RF CONNECTIONS

RF Connections

RF Jack	Name	Function	Limits
J1	Rx Out	Receive signal out	
J2	FB Out	Feedback for DPD, from PA, before circulator or filter	~38 dB below RF output level.
J3	Tx In	Transmit signal in	Max 0 dBm Peak, -10 dBm Avg.
J5	Tx Out	Transmit/Receive antenna port	-15 dBm max Receive, +39 dBm Transmit.



RapidRF Quick Start

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QUICK START: HARDWARE REQUIREMENTS

Power Supplies

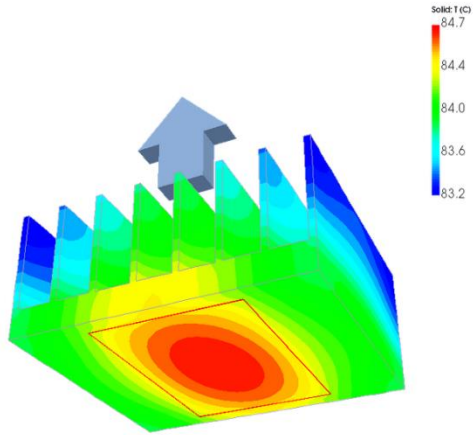
- 24-32 V, 1 A regulated supply
  - The PSU should be either high-speed or well decoupled at the device as there are significant current spikes in normal operation. A 1000 µF aluminum electrolytic capacitor is suggested.
- 5 V, 250 mA regulated supply
  - This supply is for the bias controller and the linear regulators that supply pre-driver and receiver functions.

Heatsink

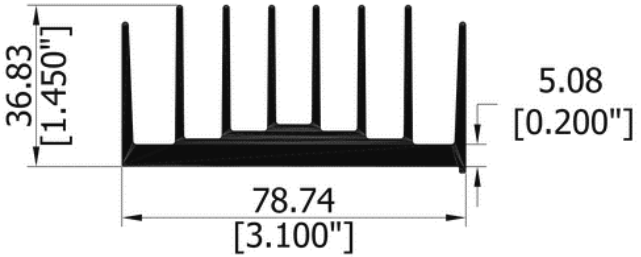
- The RapidRF board will dissipate up to 15 W in normal operation. The heat spreader included is not adequate to dissipate such power. A suitable heatsink must be attached to the heat spreader with a thermal interface material like silicone thermal compound.
- The suggested heatsink is 78 mm^2 × 36 mm high from R-Theta/Merson. Many other configurations are possible.

Transmit Receive and PA Enable Control

- For static testing jumpers may be used between control pins and the 1.8 V pin on the control connector.
- Logic levels for external controls must not exceed 2 V and cannot be clamped to the 1.8 V pins.
- Care must be taken to ensure that transmit power is not applied when the transmit/receive switch is in receive mode (low). Failure to do so may cause damage to the pre-amplifier module.



Thermal example:
40ºC ambient convection only



Heatsink example

QUICK START: POWER SEQUENCING

Power Sequencing

- Be sure to put the RapidRF board in standby mode, with both transmit and receive modes disabled before applying power.
- For transmit power down, remove the RF signal and put it in receive mode prior to removing either supply.
- The supply sequence in receive mode is not critical.

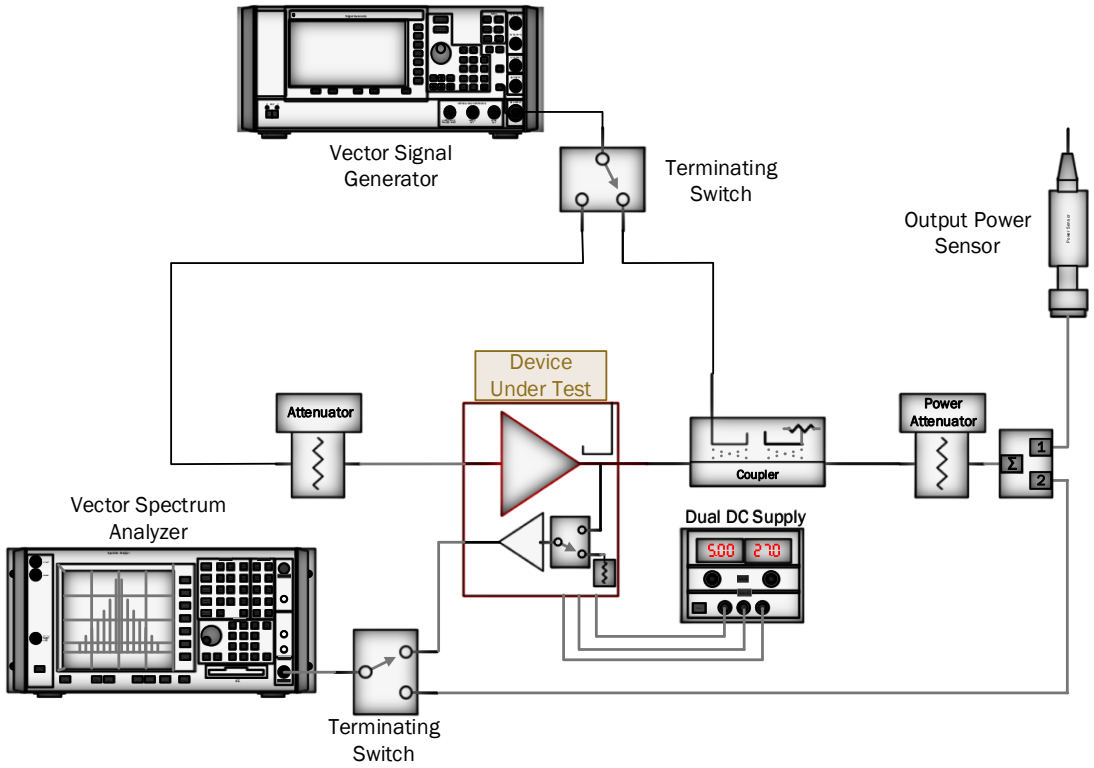
Setting Bias

- Bias controller is pre-programmed so setting of idle current is not necessary.

QUICK START: RECEIVE PATH

Receive Setup

1. Mount RapidRF board on heatsink.
2. Float or connect the PA enable terminal to ground.
3. Connect the TR switch terminal to 1.8 V (via a jumper or external supply).
4. Set the signal generator to -100 dBm and then disable RF.
5. Connect Tx/Rx In port to through coupler to attenuator.
6. Connect the signal generator to the coupler forward power port (see Setup figure).
7. Connect the analyzer to the Rx output port (see Setup figure).
8. Connect the 5 V supply.
9. Turn on the 5 V supply and note the current. It should be ~100 mA. If not, check the TR switch pin status.
10. Turn on the signal generator and slowly raise the power until the desired output is reached, taking care not to exceed -15 dBm.

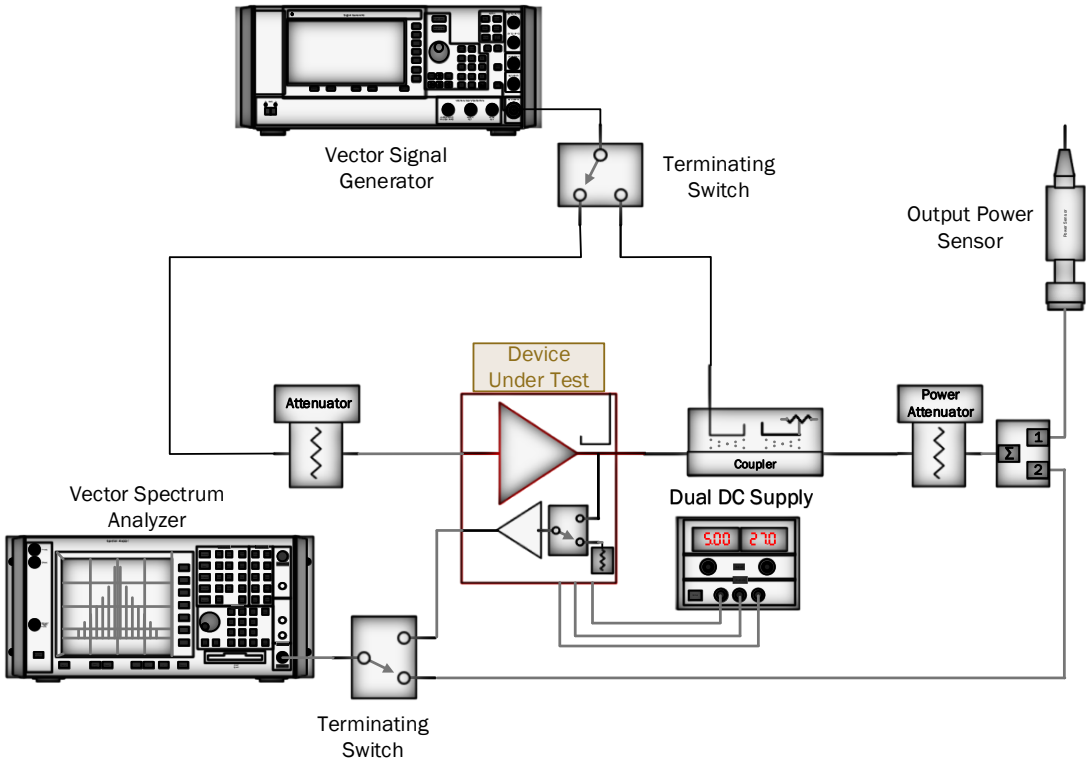


Receive Test Setup

QUICK START: TRANSMIT PATH

Transmit Setup

1. Mount RapidRF board on a heatsink capable of dissipating up to 15 W.
2. Set the signal generator to -50 dBm, or less, and then disable RF.
3. Connect the signal generator to Tx In of the RapidRF (see Setup figure).
4. Connect Tx/Rx In port to through coupler to 10 W attenuator (see Setup figure).
5. Terminate the Rx Output port and Feedback Out port.
6. Float or connect the TR switch terminal to ground.
7. Connect the 5 V supply.
8. Connect the 24-32 V supply.
9. Turn on the 5 V supply and note current. It should be less than 70 mA. If ~100 mA check TR switch status. Pin voltage should be less than .1 V.
10. Turn on the 24 V supply. The initial current should be close to 0 mA.
11. Connect the PA enable terminal to 1.8 V (via a jumper or external supply).
12. Check the 24 V supply current. It should be less than 100 mA.
13. Turn on the signal generator and slowly raise power taking care to never to exceed -15 dBm average power after input attenuator until the desired output is reached.

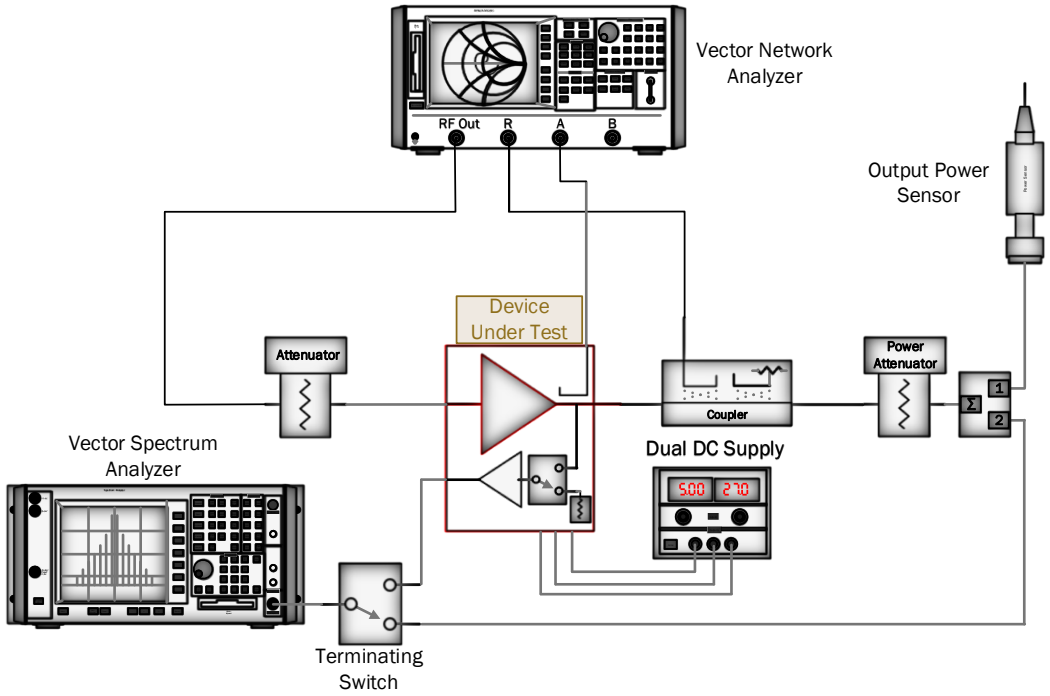


Transmitter Test Setup

QUICK START: FEEDBACK

Feedback Test Setup

1. Mount RapidRF board on a heatsink capable of dissipating up to 15 W.
2. Set the network analyzer output to -50 dBm, or less, after input attenuator.
3. Connect the signal generator to Tx In of the RapidRF board (see Setup figure).
4. Connect Tx/Rx In port to through coupler to 10 W attenuator (see Setup figure).
5. Terminate Rx Output port and Feedback Out port.
6. Float or connect TR switch terminal to ground.
7. Connect the 5 V supply.
8. Connect the 24-32 V supply (depending on model of RapidRF)
9. Turn on the 5 V supply and note current. It should be less than 70 mA. If ~100 mA check the TR switch status. Pin voltage should be less than 0.1 V.
10. Turn on the 24 V supply. The initial current should be close to 0 mA.
11. Connect the PA enable terminal to 1.8 V (via a jumper or external supply).
12. Check the 24 V supply current. It should be less than 100 mA.
13. Turn on the signal generator and slowly raise the power until the desired output is reached taking care to never exceed -15 dBm average power.



Predistortion Feedback Test Setup

REVISION HISTORY

- The following table summarizes revisions to the content of the RAPIDRF-26E39 design overview file.

Revision	Date	Description
0	May 2021	• Initial release

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