UM11303

KITVR55-FSSKTEVM evaluation board

Rev. 1 — 4 November 2019 **User guide**

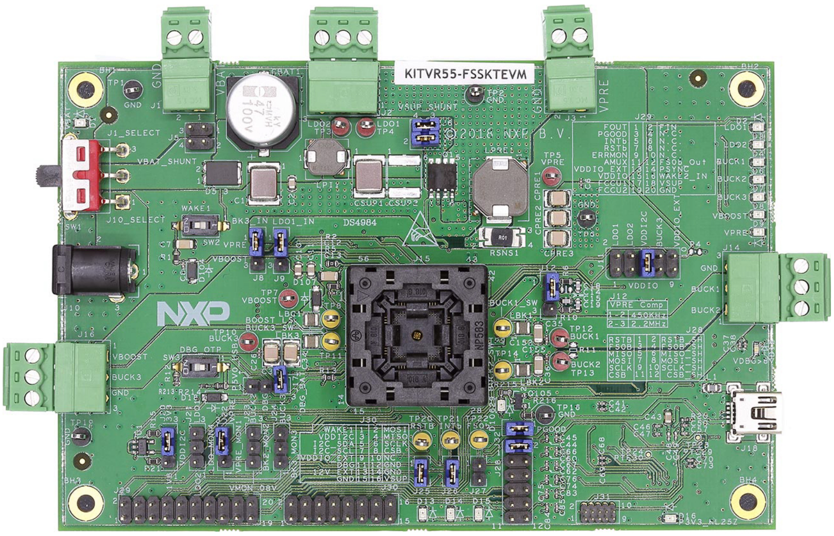

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Figure 1. KITVR55-FSSKTEVM

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This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

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1 Introduction

This document is the user guide for the KITVR55-FSSKTEVM evaluation board. This document is intended for the engineers involved in the evaluation, design, implementation, and validation of VR5500 high voltage PMIC with multiple SMPS and LDO.

The scope of this document is to provide the user with information to evaluate the VR5500 high voltage PMIC with multiple SMPS and LDO. This document covers connecting the hardware, installing the software and tools, configuring the environment and using the kit.

The KITVR55-FSSKTEVM enables development on VR5500 device. The kit can be connected to the FlexGUI software which allows you to play with registers, try OTP configurations, and burn the part.

The device can be placed and removed easily from the board by using the socket. The device OTP can be burned three times, which provides a good flexibility.

2 Finding kit resources and information on the NXP website

NXP Semiconductors provides online resources for this evaluation board and its supported device on http://www.nxp.com.

The information page for KITVR55-FSSKTEVM evaluation board is at http://www.nxp.com/KITVR55-FSSKTEVM. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a **Getting Started** tab. The **Getting Started** tab provides quick-reference information applicable to using the KITVR55-FSSKTEVM evaluation board, including the downloadable assets referenced in this document.

2.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, ask and answer technical questions, and receive input on just about any embedded design topic.

The NXP community is at http://community.nxp.com.

3 Getting ready

Working with the KITVR55-FSSKTEVM requires the kit contents, additional hardware, and a Windows PC workstation with installed software.

3.1 Kit contents

- Assembled and tested evaluation board in an anti-static bag
- 3.0 ft USB-STD A to USB-B-mini cable
- Two connectors, terminal block plug, 2 pos., str. 3.81 mm
- Three connectors, terminal block plug, 3 pos., str. 3.81 mm
- Jumpers mounted on board

3.2 Additional hardware

In addition to the kit contents, the following hardware is necessary or beneficial when working with this kit.

- Power supply with a range of 8.0 V to 60 V and a current limit set initially to 1.0 A

3.3 Windows PC workstation

This evaluation board requires a Windows PC workstation. Meeting these minimum specifications should produce great results when working with this evaluation board.

- USB-enabled computer with Windows 7 or Windows 10

3.4 Software

Installing software is necessary to work with this evaluation board. All listed software is available on the information page of the evaluation board at http://www.nxp.com/KITVR55-FSSKTEVM or from the provided link.

- FlexGUI latest version
- VR5500_OTP_Config.xlsm
- Java installation https://www.oracle.com/technetwork/java/javase/downloads/jre8-downloads-2133155.html

4 Getting to know the hardware

The KITVR55-FSSKTEVM provides flexibility to play with all the features of the device and make measurements on the main part of the application. The KL25Z MCU installed on the board, combined with the FlexGUI software allows access to the registers in read and write mode. All regulators are accessible through connectors. Nonuser signals, like DC-to-DC switcher node are mapped on test points. Digital signals (I2C, RSTB, etc.) are accessible through connectors. Pin WAKE1 has a switch to control (ignition) them. A V_{BAT} switch is available to power on or off the device.

The main purpose of this kit is to burn the OTP configuration. This kit can be operated in Emulation mode or in OTP mode. In Emulation mode, as long as the power is supplied, the board configuration stays valid. The OTP mode uses the fused configuration. The device can be fused three times. In OTP mode, the device always starts with the fused configuration, except if the user wants to overwrite OTP configuration using Emulation mode. This board is able to fuse the OTP without any extra tools or board.

Note: *Due to the socket, this kit is not optimized for performance measurement or current higher than 1.0 A.*

4.1 Kit overview

The KITVR55-FSSKTEVM is a hardware evaluation tool that allows OTP burning. Due to the socket, the VR5500 part can be configured without the need to solder it. The device can be programmed three times (see Section 7.3).

An Emulation mode is possible to test as many configurations as needed.

An external LDO provides VDDI2C voltage with a choice of 1.8 V or 3.3 V (default). VDDIO is assigned by default to VDDI2C. From USB voltage, an external DC-to-DC generates the OTP programming voltage (8.0 V) without any need for an external power supply.

4.1.1 KITVR55-FSSKTEVM features

- VBAT power supply connectors (Jack and Phoenix)
- VPRE output capability up to 1.0 A (socket limit)
- VBUCK1/2 in Standalone mode (default) or Multiphase mode
- VBUCK3
- VBOOST 5.0 V or 5.74 V
- LDO1 and LDO2, from 1.1 V to 5.0 V
- Ignition key switch
- Embedded USB connection for easy connection to software GUI (access to I^2C-bus, IOs, RSTB, INTB, Debug, MUX_OUT, regulators)
- LEDs that indicate signal or regulator status
- Support OTP fuse capabilities
- USB connection for register access, OTP emulation, and programming
- Voltage monitoring jumper setting

Note: *Due to the socket, all current capabilities are limited to 1.0 A.*

4.1.2 VMON1 board configuration

VMON1 is a general-purpose voltage monitoring input. VMON1 can be connected to VPRE, LDO1, LDO2, BUCK3, BUCK2 (in case BUCK2 is not used in multiphase), or even an external regulator. This kit is delivered with VMON1 assigned to VPRE, the bridge resistor set for 3.3 V.

Due to the jumpers, VMON1 can be tied to a 0.8 V to force a good voltage at pin level. It behaves like hardware disabling and makes debug easy in some cases.

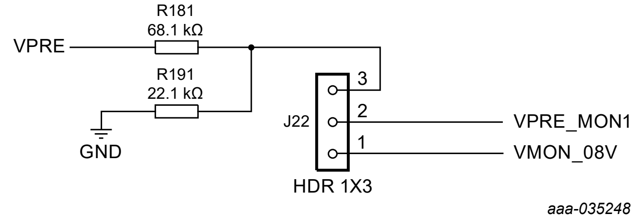


Figure 2. VMON1 configuration

4.1.3 VPRE compensation network

This board is delivered with a VPRE compensation network defined for VPRE 4.1 V at 450 kHz. All other VPRE configurations require a new calculation for these components.

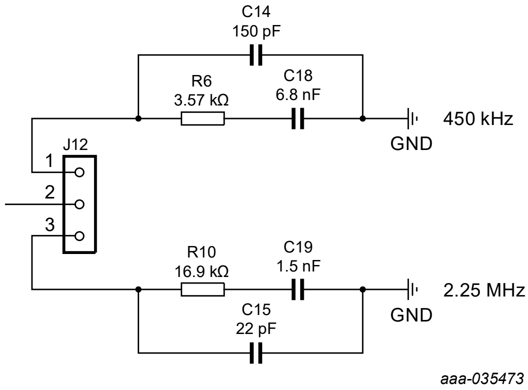


Figure 3. VPRE compensation network

Table 1. Compensation network

Components	VPRE 450 kHz	VPRE 2.2 MHz
C18/C19	6.8 nF	1.5 nF
C14/C15	150 pF	22 pF
R6/R10	3.57 kΩ	16.9 kΩ

4.1.4 BUCK1 and BUCK2 multiphase configuration

The board is designed to work independently with BUCK1 and BUCK2. Due to R11 and R145, it is possible to connect both connectors together and work in multiphase.

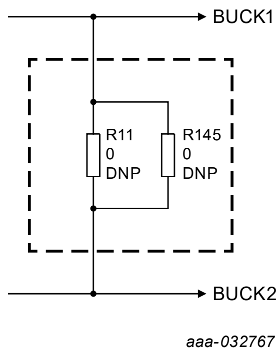


Figure 4. BUCK1 and BUCK2 multiphase configuration

4.1.5 VDDI2C

As an option, an external LDO is provided to feed VDDI2C. This LDO can also be used to feed VDDIO, which is the default implementation.

The I^2C-bus is compatible with 1.8 V or 3.3 V, while VDDIO is compatible with 3.3 V and 5.0 V. For this reason, the LDO default configuration is 3.3 V. The LDO is supplied by 5.0 V coming from the USB.

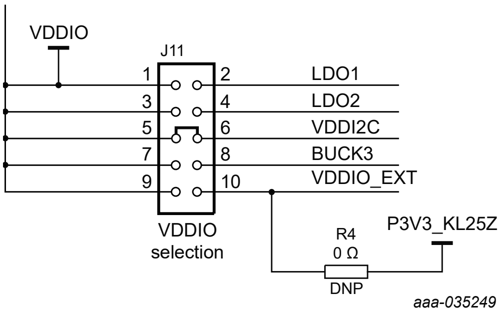


Figure 5. VDDIO selection

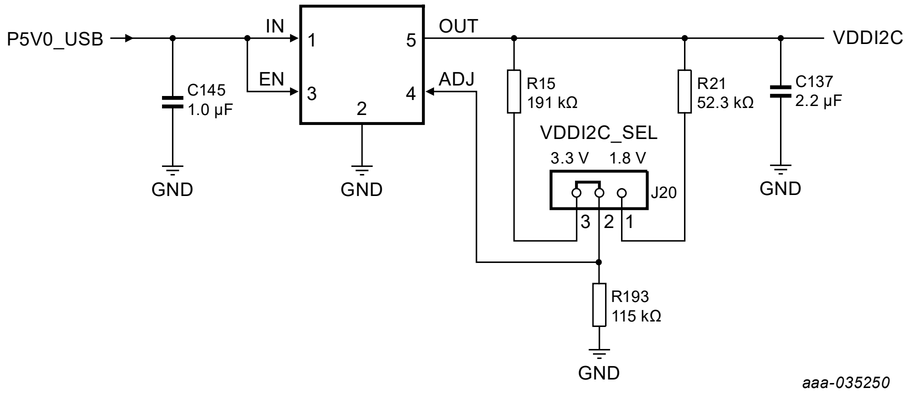


Figure 6. VDDI2C supply

4.2 Device OTP user configuration

It is recommended to learn about OTP before operating with the device. The device has a high level of flexibility due to parameter configuration available in the OTP, which impacts the functionality of the device. It is key to understand how OTP parameters can be programmed, the interaction with mirror registers and the VR5500 SoC.

The OTP related operations can be performed either in Emulation mode, where the product uses a given configuration as long as power supply is not switched off or from OTP fuse content that is valid even after a power down/power up sequence.

4.2.1 OTP and mirrors registers

There are two OTP blocks in the device. One is for the main section, and the other for the fail-safe. During configuration, each of them are using dedicated sectors. The OTP configuration scheme is shown in Figure 7 (same implementation for main and fail-safe).

The device can be fused three times using mirror registers. The user can first load the mirror register content with the desired contents, then decide either to use the device in Emulation mode or to burn the next sector. The first sector to be burned is S1, the second S1bis, and the third S1ter. FlexGUI automatically manages the next sector to be burned. It is not possible to revert to the previous sector. When the user reaches the sector S1ter, there no other possibility for burn, however emulation mode is still available.

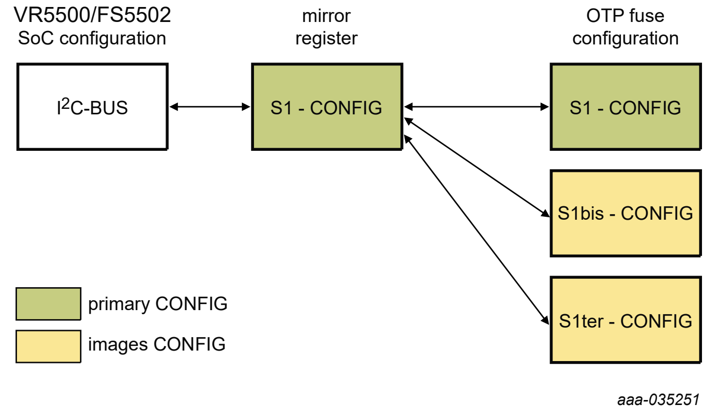


Figure 7. OTP configuration

At boot, the content of the valid sector is loaded into the Mirror Register Sector 1. The mirror register content is accessible from FlexGUI by using specific I^2C-bus commands. The mirror configuration is managed by the FlexGUI, which eases the access.

4.2.2 OTP hardware implementation

To work in OTP emulation or OTP programming, it is required to start the device in Debug mode.

Figure 8 shows the sequence to be followed to enter in Debug mode. The voltage sequence on the kit is done using switches installed on the board, while the OTP registers configuration is managed by the FlexGUI. It is described in detail in the following sections.

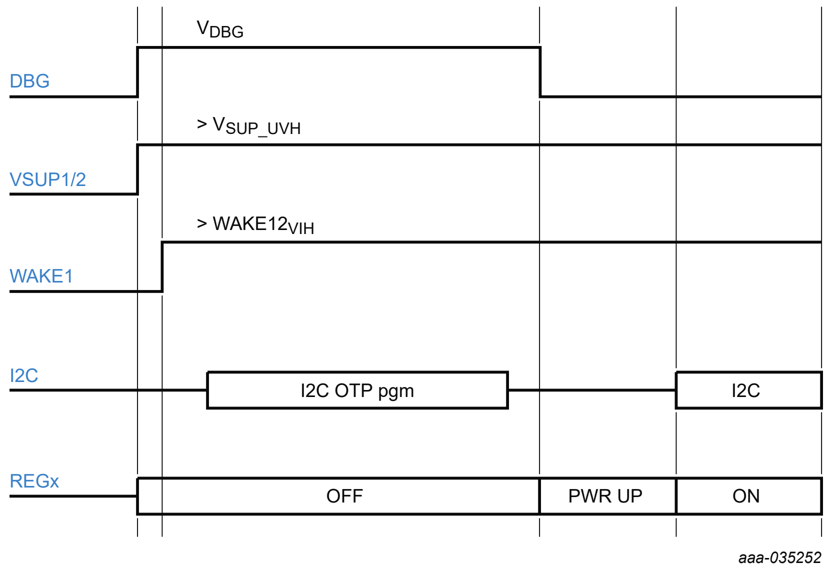


Figure 8. Debug mode entry

Figure 9 shows the hardware kit implementation.

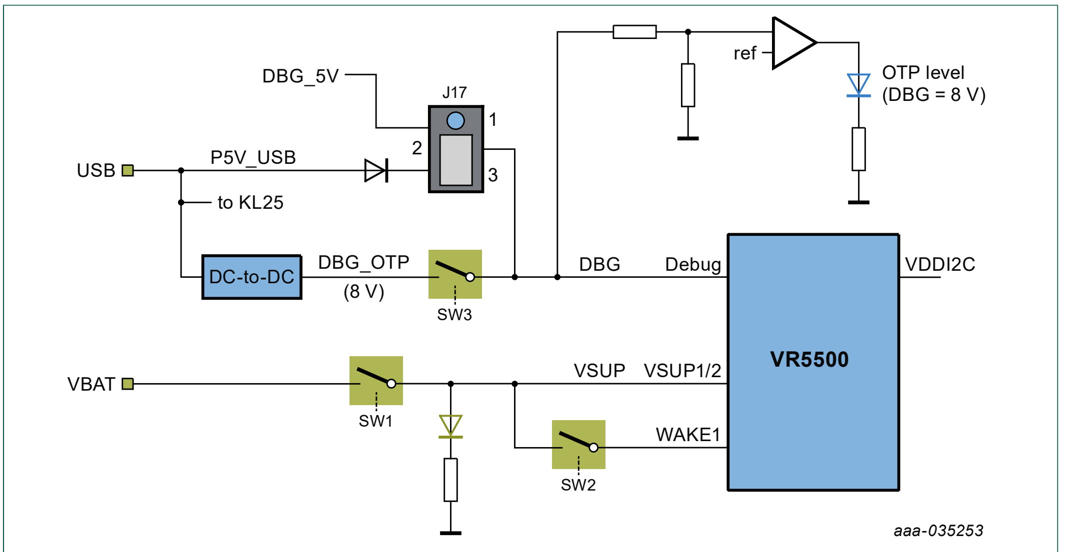
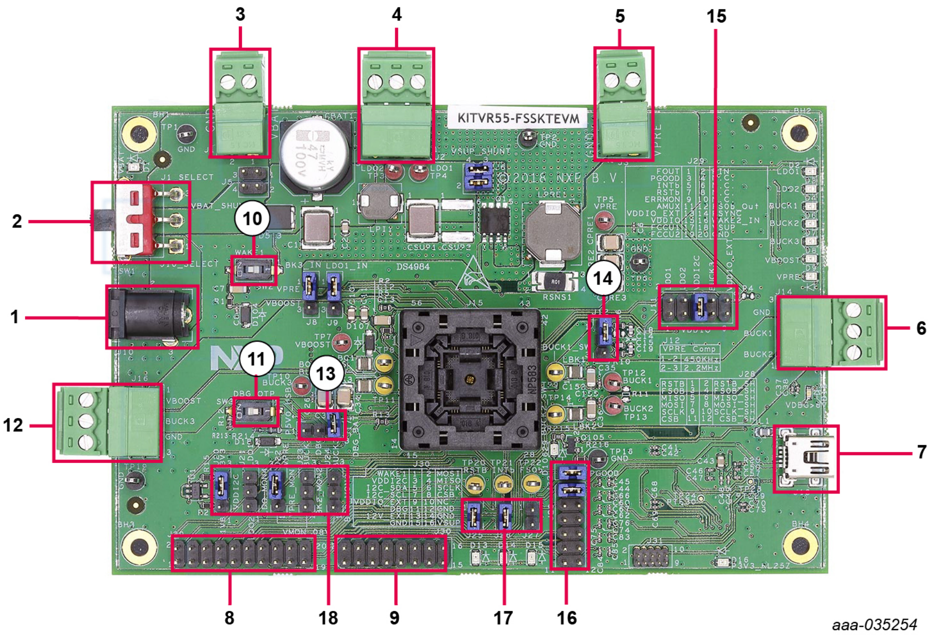


Figure 9. OTP hardware implementation

4.3 Kit featured components

Figure 10 identifies important components on the board and Table 2 provides additional details on these components.



1. V_{BAT} Jack connector
2. V_{BAT} three position switch
3. V_{BAT} Phoenix connector
4. LDO1/LDO2 power supplies
5. VPRE power supply
6. BUCK1/BUCK2 power supply
7. USB connector (for FlexGUI control)
8. Debug connectivity
9. Programming
10. WAKE1 switch
11. OTP burning voltage switch
12. VBOOST and BUCK3 power supply
13. Debug voltage source
14. Compensation network selection
15. VDDIO selection
16. RSTB connection to MCU
17. RSTB and INTb signals
18. VMON1 and VDDI2C selection

Figure 10. Evaluation board featured component locations

Table 2. Evaluation board component descriptions

Number	Description
1	V_{BAT} Jack connector
2	V_{BAT} three position switch • Left position: board supplied by Jack connector • Middle position: board not supplied • Right position: board supplied by Phoenix connector
3	V_{BAT} Phoenix connector
4	LDO1/LDO2 power supplies
5	VPRE power supply
6	BUCK1/BUCK2 power supply
7	USB connector (for FlexGUI control)
8	debug connectivity; access to: • VSUP, GND • FOUT/FIN • PGOOD/RST • WAKE2 • PSYNC, AMUX • VMON1
9	programming • I^2C-bus • Pin DBG • VPRE, VSUP, GND
10	WAKE1 switch
11	OTP burning voltage switch
12	VBOOST and BUCK3 power supply
13	debug voltage source either from USB (recommended) or from VSUP
14	VPRE compensation network selection, either 2.2 MHz or 450 kHz
15	VDDIO source from device regulators or external sources
16	RSTB can be disconnected between device and MCU
17	RSTB and INTb signals available here (device pin level)
18	allows user to select VMON1 from regulators or a fix 0.8 V; VDDI2C can be selected either 1.8 V or 3.3 V

4.3.1 VR5500: high voltage PMIC with multiple SMPS and LDO

4.3.1.1 General description

The VR5500 is an automotive high-voltage multi-output power supply integrated circuit, with focus on radio, V2X, and infotainment applications. It includes multiple switch mode and linear voltage regulators. It offers external frequency synchronization input and output, for optimized system EMC performance.

Several device versions are available, offering choice in number of output rails, output voltage setting, operating frequency, and power up sequencing, to address multiple applications.

4.3.1.2 Features

- 60 V DC maximum input voltage for 12 V and 24 V applications
- VPRE synchronous buck controller with external MOSFETs. Configurable output voltage, switching frequency, and current capability up to 10 A peak.
- Low voltage integrated synchronous BUCK1 converter, dedicated to MCU core supply with SVS capability. Configurable output voltage and current capability up to 3.6 A peak.
- Low voltage integrated synchronous BUCK2 converter. Configurable output voltage and current capability up to 3.6 A peak. Multi-phase capability with BUCK1 to extend the current capability up to 7.2 A peak on a single rail. Static voltage scaling capability.
- Low voltage integrated synchronous BUCK3 converter. Configurable output voltage and current capability up to 3.6 A peak.
- BOOST converter with integrated low-side switch. Configurable output voltage and max input current up to 1.5 A peak.
- EMC optimization techniques including SMPS frequency synchronization, spread spectrum, slew rate control, manual frequency tuning
- Two linear voltage regulators for MCU IOs and ADC supply, external physical layer. Configurable output voltage and current capability up to 400 mA DC.
- OFF mode with very low sleep current (10 µA typ)
- Two input pins for wake-up detection and battery voltage sensing
- Device control via I^2C-bus interface with CRC
- Power synchronization pin to operate two VR5500 devices or VR5500 plus an external PMIC
- Three voltage monitoring circuits, dedicated interface for MCU monitoring, power good, reset, and interrupt outputs
- Configuration by OTP programming. Prototype enablement to support custom setting during project development in engineering mode.

4.3.2 Indicators

The following LEDs are provided as visual output devices for the evaluation board:

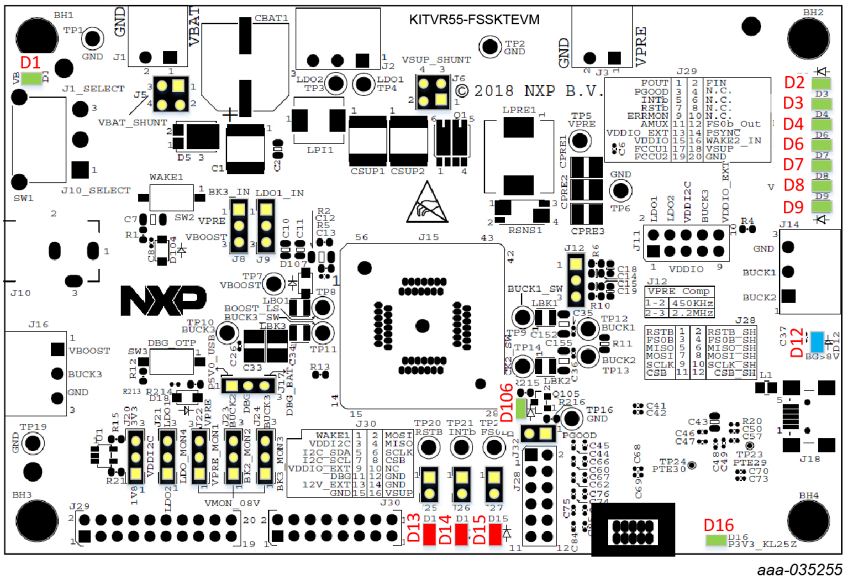


Figure 11. Evaluation board indicator locations

Table 3. Evaluation board indicator descriptions

Label	Name	Color	Description
D1	V_{BAT}	green	V_{BAT} on
D2	LDO1	green	LDO1 on
D3	LDO2	green	LDO2 on
D4	BUCK1	green	BUCK1 on
D6	BUCK2	green	BUCK2 on
D7	BUCK3	green	BUCK3 on
D8	VBOOST	green	VBOOST on
D9	V_{PRE}	green	V_{PRE} on
D12	DBG > 8.0 V	blue	DBG pin voltage > 8.0 V (OTP programming)
D13	RSTB	red	RSTB asserted (logic level = 0)
D14	INTb	red	INTb asserted (logic level = 0)
D15	FS0b	red	not available
D16	P3V3_KL25	green	P3V3_KL25 on
D106	PGOOD	green	PGOOD released

4.3.3 Connectors

Figure 12 shows the location of connectors on the board.

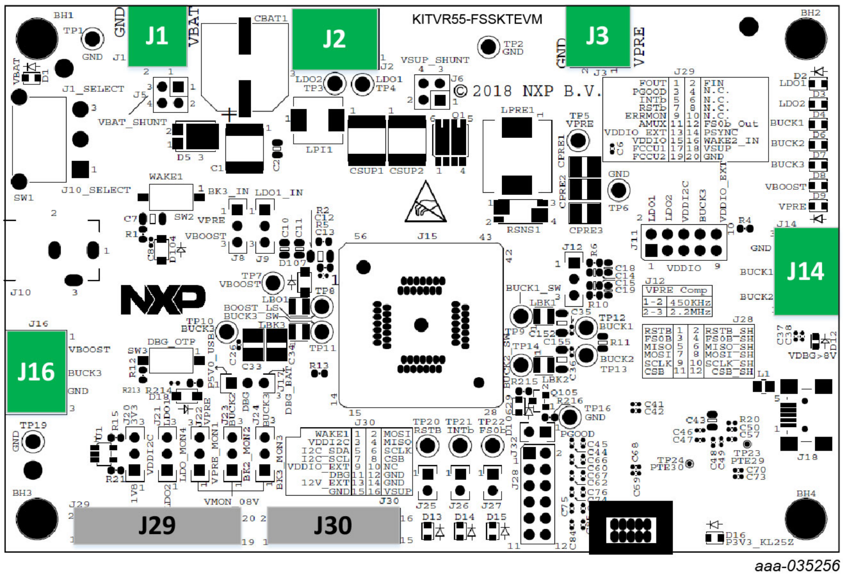


Figure 12. Evaluation board connector locations

4.3.3.1 V_{BAT} connector (J1)

V_{BAT} connects to the board through Phoenix connector (J1).

Table 4. V_{BAT} Phoenix connector (J1)

Schematic label	Signal name	Description
J1-1	V_{BAT}	battery voltage supply input
J1-2	GND	ground

4.3.3.2 Output power supply connectors

Table 5. BUCK1/BUCK2 connector (J14)

Schematic label	Signal name	Description
J14-1	BUCK2	BUCK2 power supply output
J14-2	BUCK1	BUCK1 power supply output
J14-3	GND	ground

Table 6. VBOOST/BUCK3 connector (J16)

Schematic label	Signal name	Description
J16-1	VBOOST	VBOOST output
J16-2	BUCK3	BUCK3 power supply output
J16-3	GND	ground

Table 7. LDO1/LDO2 connector (J2)

Schematic label	Signal name	Description
J2-1	LDO1	LDO1 power supply output
J2-2	LDO2	LDO2 power supply output
J2-3	GND	ground

Table 8. VPRE connector (J3)

Schematic label	Signal name	Description
J3-1	VPRE	VPRE power supply output
J3-2	GND	ground

4.3.3.3 Debug connector (J29)

Table 9. Debug connector (J29)

Schematic label	Signal name	Description
J29-1	FOUT	frequency synchronization output
J29-2	FIN	frequency synchronization input
J29-3	PGOOD	power GOOD
J29-4	n.c.	not connected
J29-5	INTb	interrupt, active LOW
J29-6	n.c.	not connected
J29-7	RSTB	reset, active LOW
J29-8	n.c.	not connected
J29-9	n.c.	not connected
J29-10	n.c.	not connected
J29-11	AMUX	analog multiplexer
J29-12	n.c.	not connected
J29-13	VDDIO_EXT	VDDIO external reference
J29-14	PSYNC	power synchronization
J29-15	VDDIO	VDDIO used by VR5500
J29-16	WAKE2_IN	WAKE2 input
J29-17	n.c.	not connected
J29-18	VSUP	VSUP power supply
J29-19	n.c.	not connected
J29-20	GND	ground

4.3.3.4 Program connector (J30)

Table 10. Program connector (J30)

Schematic label	Signal name	Description
J30-1	WAKE1	WAKE1 input
J30-2	n.c.	not connected
J30-3	VDDI2C	VDDI2C voltage
J30-4	n.c.	not connected
J30-5	I2C_SDA	I^{2}C-bus serial data
J30-6	n.c.	not connected
J30-7	I2C_SCL	I^{2}C-bus serial clock
J30-8	n.c.	not connected
J30-9	n.c.	not connected
J30-10	n.c.	not connected
J30-11	DBG	connected to pin DBG
J30-12	GND	ground
J30-13	n.c.	not connected
J30-14	GND	ground
J30-15	GND	ground
J30-16	VSUP	connected to VSUP pin

4.3.4 Test points

The following test points provide access to various signals to and from the board.

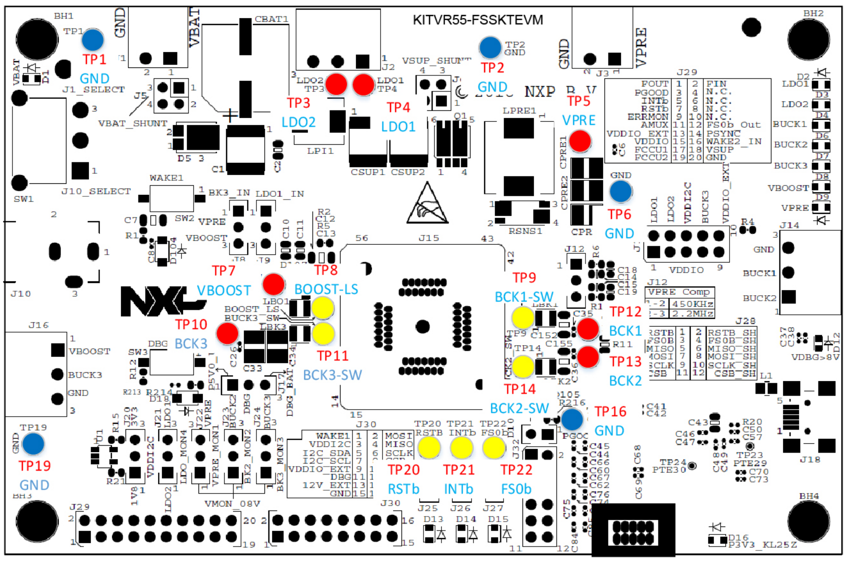


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Figure 13. Evaluation board test points

Table 11. Evaluation board test point descriptions

Test point name	Signal name	Description
TP1	GND	ground
TP2	GND	ground
TP3	LDO2	LDO2 regulator output
TP4	LDO1	LDO1 regulator output
TP5	VPRE	VPRE DC-to-DC regulator output
TP6	GND	ground
TP7	VBOOST	VBOOST DC-to-DC output
TP8	BOOST_LS	VBOOST low-side switcher
TP9	BUCK1_SW	BUCK1 switcher
TP10	BUCK3	BUCK3 DC-to-DC regulator output
TP11	BUCK3_SW	BUCK3 switcher
TP12	BUCK1	BUCK1 DC-to-DC regulator output
TP13	BUCK2	BUCK2 DC-to-DC regulator output
TP14	BUCK2_SW	BUCK2 switcher
TP16	GND	ground
TP19	GND	ground
TP20	RSTB	reset
TP21	INTb	interruption
TP22	n.c.	not connected

4.3.5 Jumpers

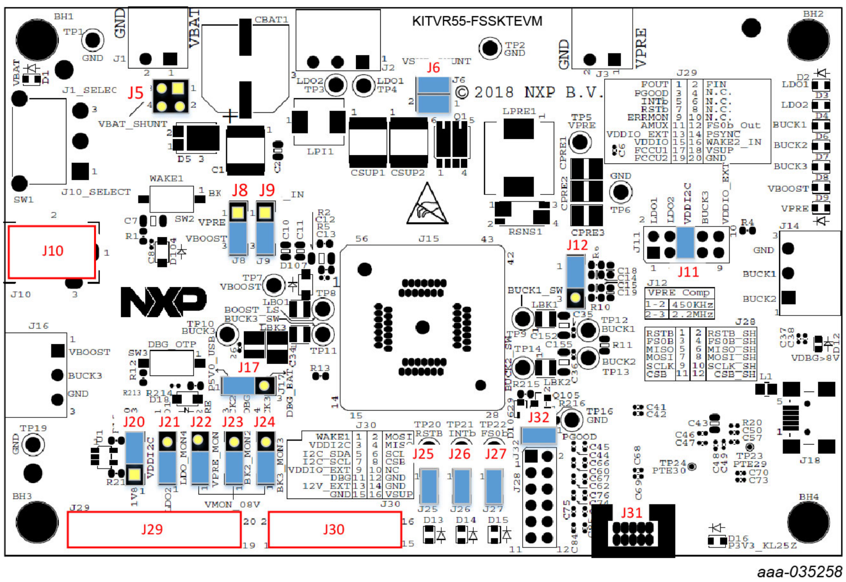

Figure 14. Evaluation board jumper locations

Table 12. Evaluation board jumper descriptions

Name	Function	Pin number	Jumper/pin function
J5	V_{BAT} shunt	1–2	shunt switch SW1 for current > 5.0 A
		3–4	shunt switch SW1 for current > 5.0 A
J6	V_{SUP} shunt	1–2	for current measurement (insert amperemeter)
		3–4	for current measurement (insert amperemeter)
J8	BUCK3 input	1–2	BUCK_INQ tied to VPRE
		2–3	BUCK_INQ tied to VBOOST
J9	LDO1 input	1–2	LDO1_IN connected to V_{PRE}
		2–3	LDO1_IN connected to VBOOST
J10	V_{BAT} Jack	Jack	used for V_{BAT} supply using Jack connector
J11	VDDIO selection	1–2	VDDIO tied to LDO1
		3–4	VDDIO tied to LDO2
		5–6	VDDIO tied to VDDI2C (provided by external regulators)
		7–8	VDDIO tied to BUCK3
		9–10	VDDIO tied to VDDIO external
J12	VPRE compensation network selection	1–2	450 kHz VPRE compensation network
		2–3	2.25 MHz VPRE compensation network
J17	debug	1–2	pin DBG tied to P5V0_USB (5.0 V provided by USB connector)
		2–3	pin DBG tied to V_{BAT} (through external protection); do not use for OTP burning
J20	VDDI2C_SEL	1–2	external regulator output 1.8 V
		2–3	external regulator output 3.3 V
J21	n.c.	1–2	n.c.
		2–3	n.c.
J22	VMON1	1–2	VMON1 tied to 0.8 V
		2–3	VMON1 tied to VPRE
J23	n.c.	1–2	n.c.
		2–3	n.c.
J24	n.c.	1–2	n.c.
		2–3	n.c.
J25	RSTB	1–2	reset LED; enabled when jumper is plugged
J26	INTb	1–2	interrupt LED; enabled when jumper is plugged
J27	n.c.	1–2	n.c.
J29	—	—	—
J30	—	—	—
J31	—	—	use only during board manufacturing
J32	PGOOD	1–2	PGOOD LED; enabled when jumper is plugged

4.3.6 Switches

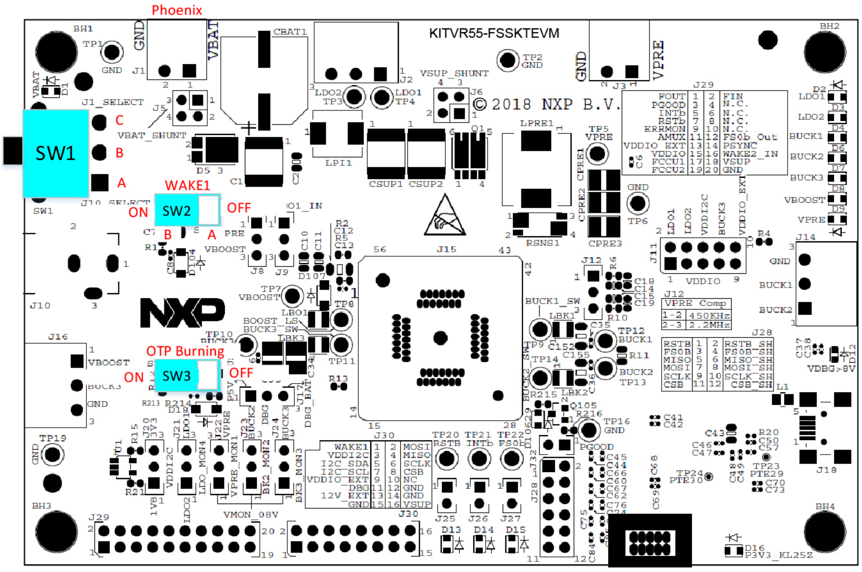

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Figure 15. Switch locations

Table 13. SW3

Position	Function	Description
RIGHT	OTP programming off	OTP burning not possible
LEFT	OTP programming on	8.0 V on DBG pin allows OTP burning (blue LED turns on to indicate this state)

Table 14. SW2

Position	Function	Description
OFF	WAKE1 open	WAKE1 pin not connected to V_{SUP}
ON	WAKE1 closed	WAKE1 pin connected to V_{SUP}

Table 15. SW1

Position	Function	Description
TOP	V_{BAT} on	V_{BAT} from J1
MIDDLE	V_{BAT} off	board not supplied
BOTTOM	V_{BAT} on	V_{BAT} from J10

4.4 Schematic, board layout and bill of materials

The schematic, board layout and bill of materials for the KITVR55-FSSKTEVM evaluation board are available at http://www.nxp.com/KITVR55-FSSKTEVM.

5 Installing and configuring software and tools

This development kit uses FlexGUI software. FlexGUI software is based on Java JRE.

Preparing the Windows PC workstation consists of three steps.

1. Install the appropriate Java SE Runtime Environment (JRE).
2. Install Windows 7 FlexGUI driver.
3. Install FlexGUI software package.

5.1 Installing the Java JRE

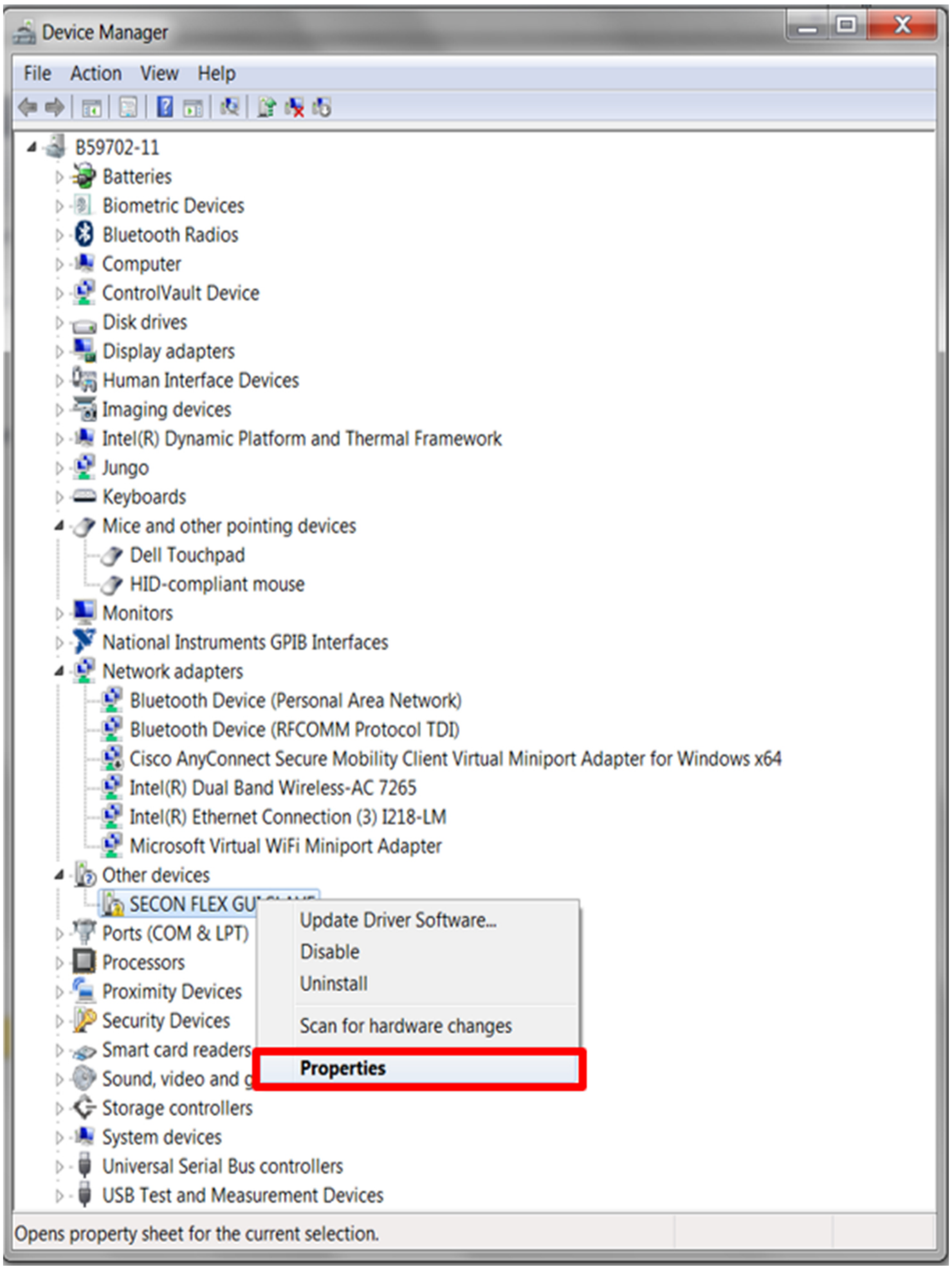
1. Download Java JRE (Java SE Runtime Environment), available at http://www.oracle.com/technetwork/java/javase/downloads/jre8-downloads-2133155.html (8u162 or newer).
2. Open the installer and follow the installation instructions.
3. Following the successful installation, restart the computer.

5.2 Installing Windows 7 FlexGUI driver

On Windows 7 PCs, a virtual COM port installation is required. Install the Windows 7 FlexGUI driver using the following procedure.

Note: *On Windows 10, it is not necessary to install virtual com port as Windows 10 uses a generic COM port driver.*

1. Connect the kit to the computer as described in Section 6
2. On the Windows PC, open the **Device Manager**.
3. In the **Device Manager** window, right-click on **SECON FLEX GUI SLAVE**, and then select **Properties**.



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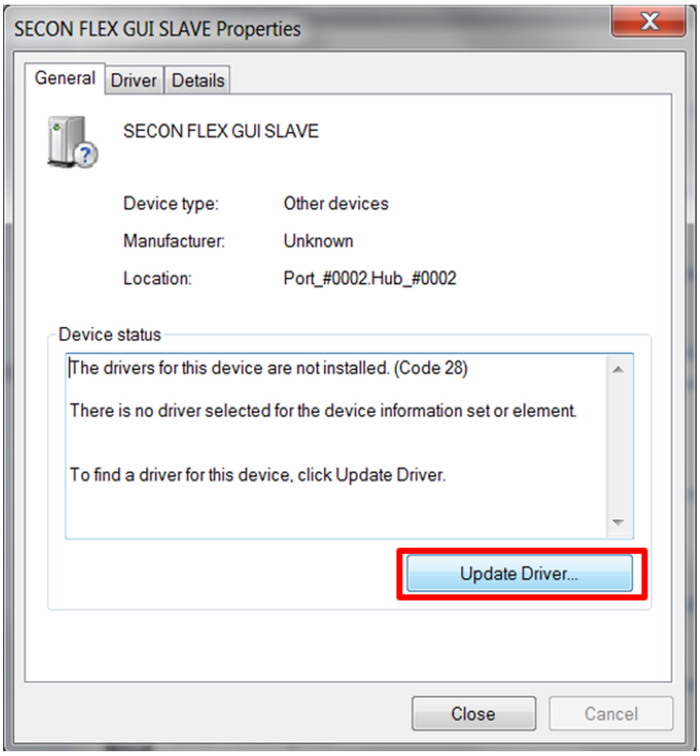
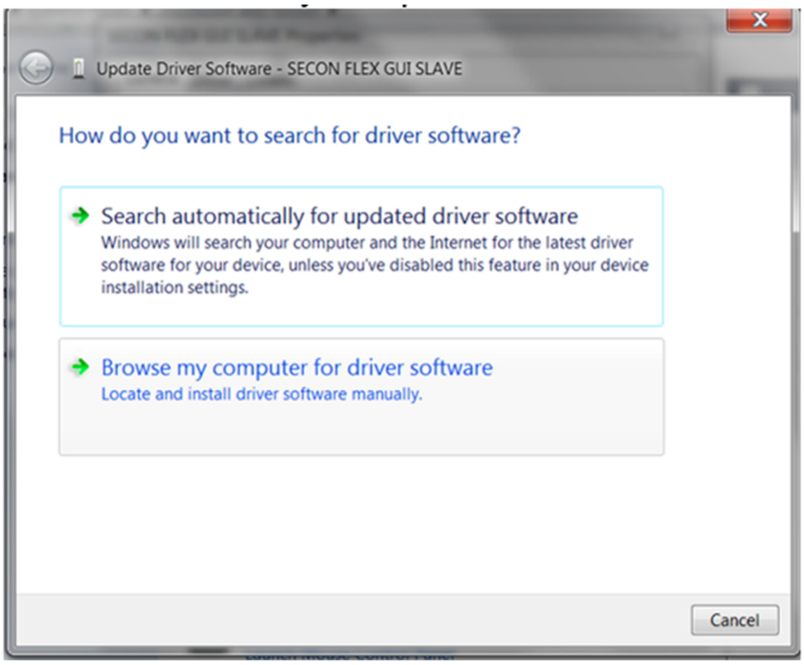
4. In the **SECON FLEX GUI SLAVE Properties** window, click **Update Driver**.



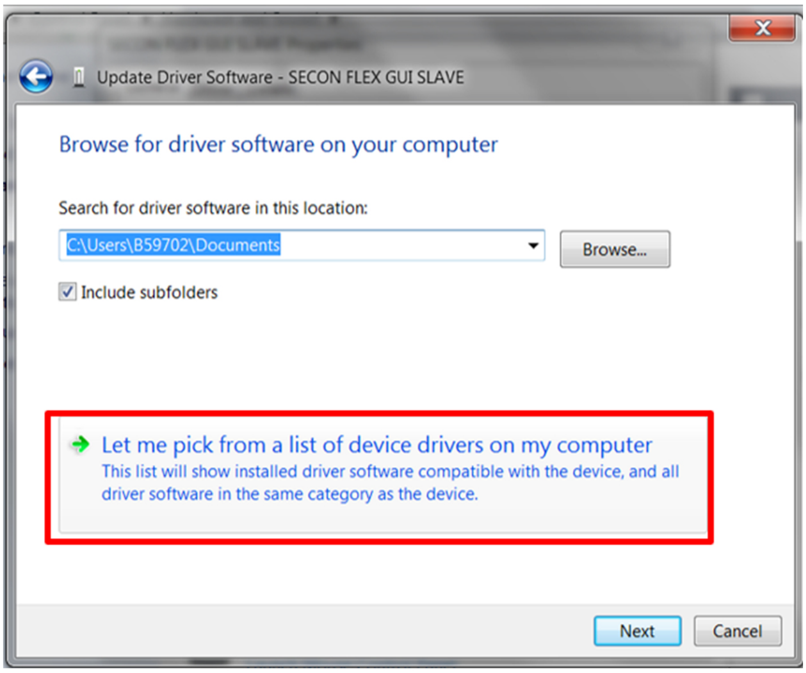
aaa-031983

5. in the **Update Software Driver window**, select **Browse my computer for driver software**.



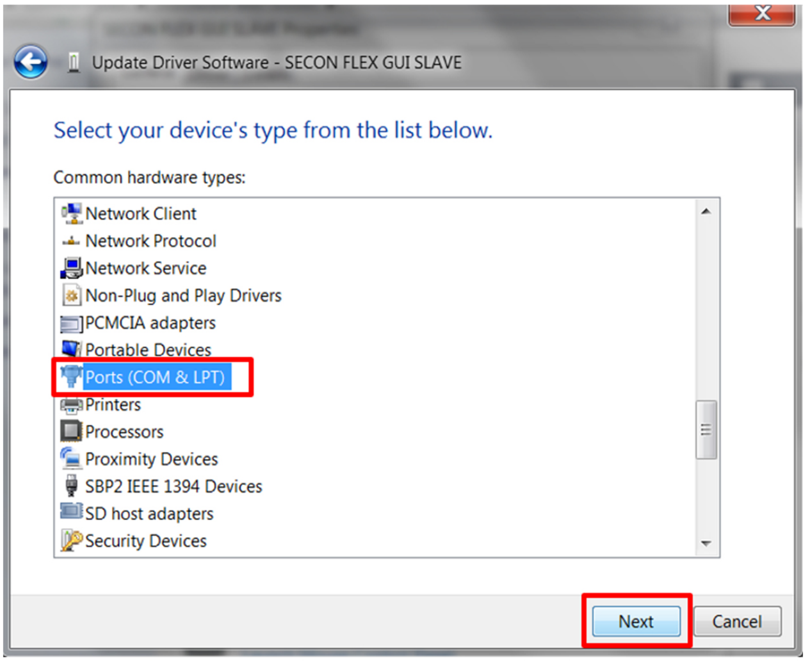
aaa-031984

6. Select **Let me pick from a list of device drivers on my computer**, and then click **Next**.



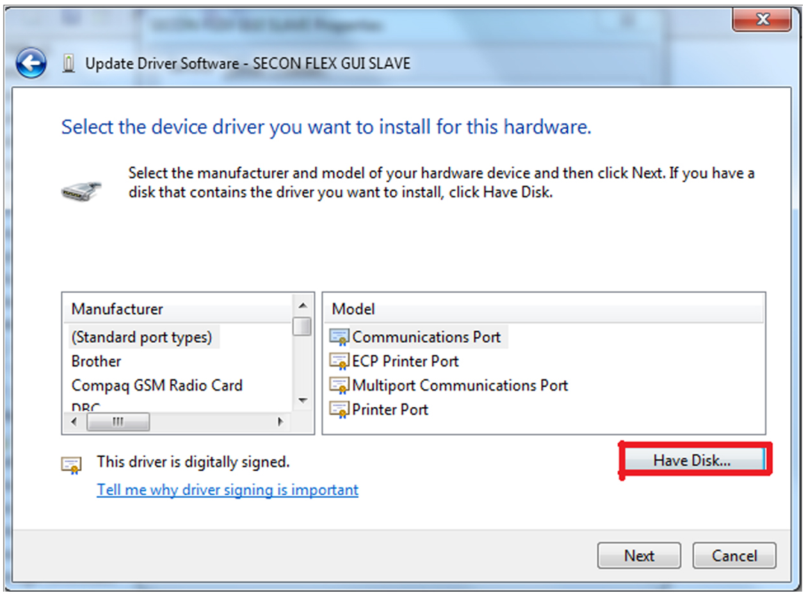
aaa-031985

7. Select **Ports (COM & LPT)** from the list, and then click **Next**.



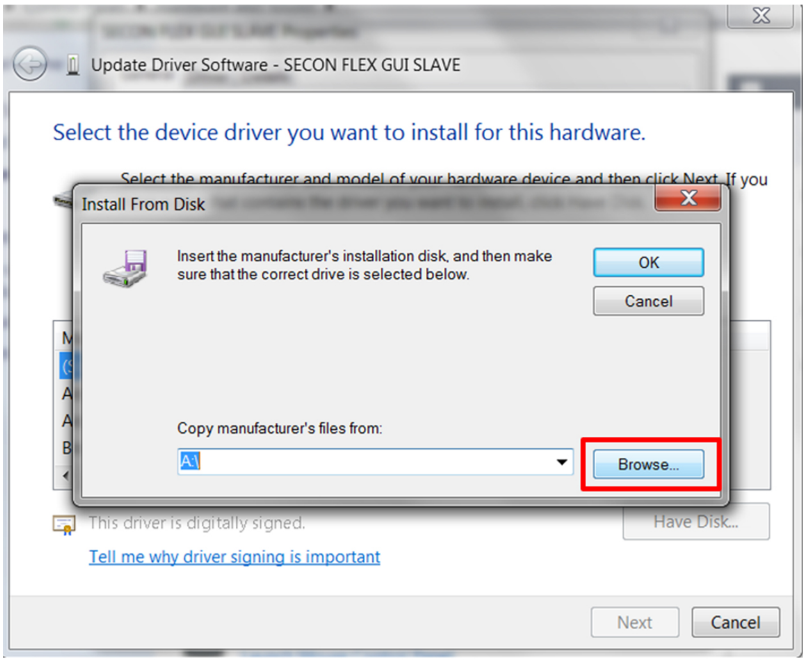
aaa-031986

8. Click **Have Disk**.



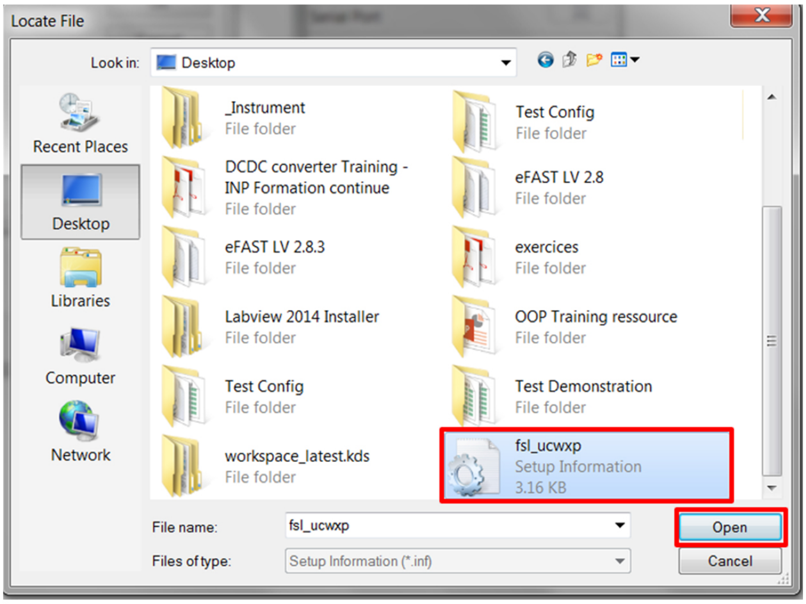
aaa-031987

9. Click **Browse**.



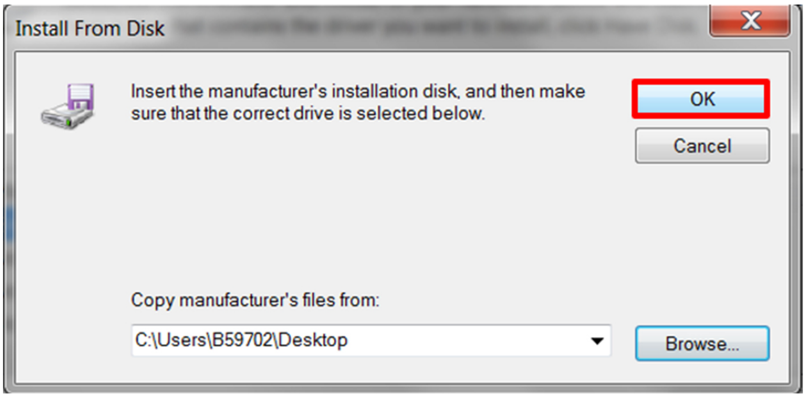
aaa-031988

10. In the **Locate File** window, locate and select **fsl_ucwxp**, and then click **Open**.



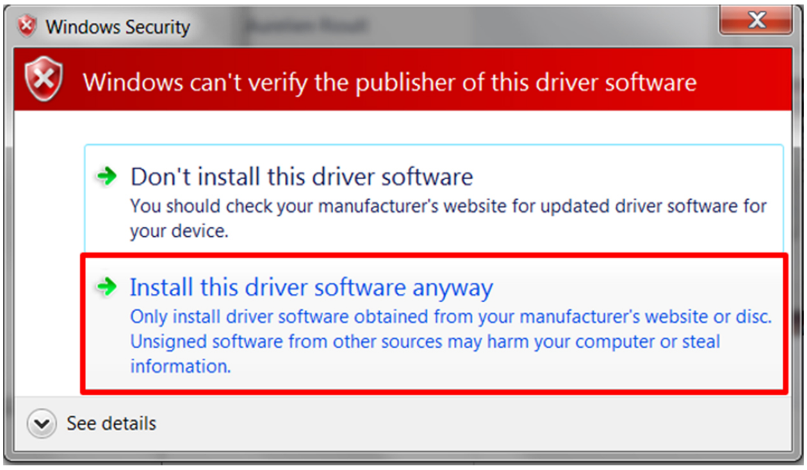
aaa-031989

11.In the **Install from Disk** window, click **OK**.



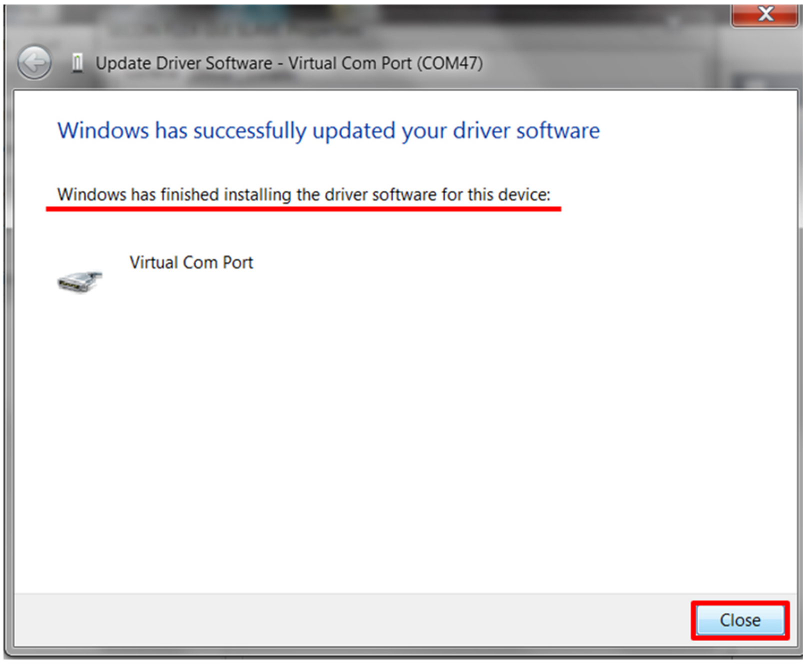
aaa-031990

12.If prompted, in the **Windows Security** window, click **Select this driver software anyway**.



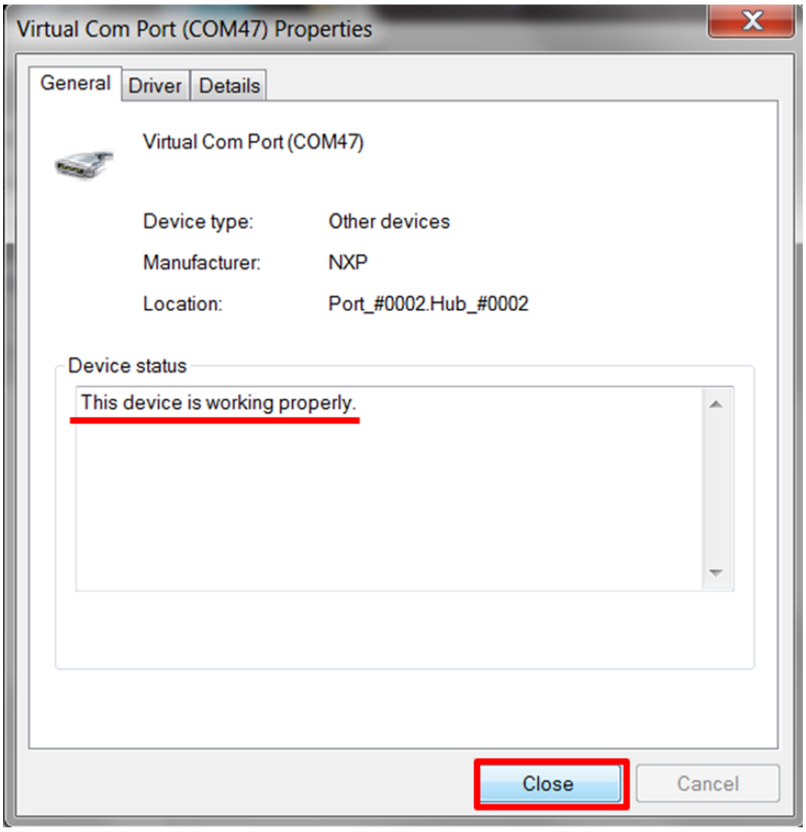
aaa-031991

13. Close the window when the installation is complete.



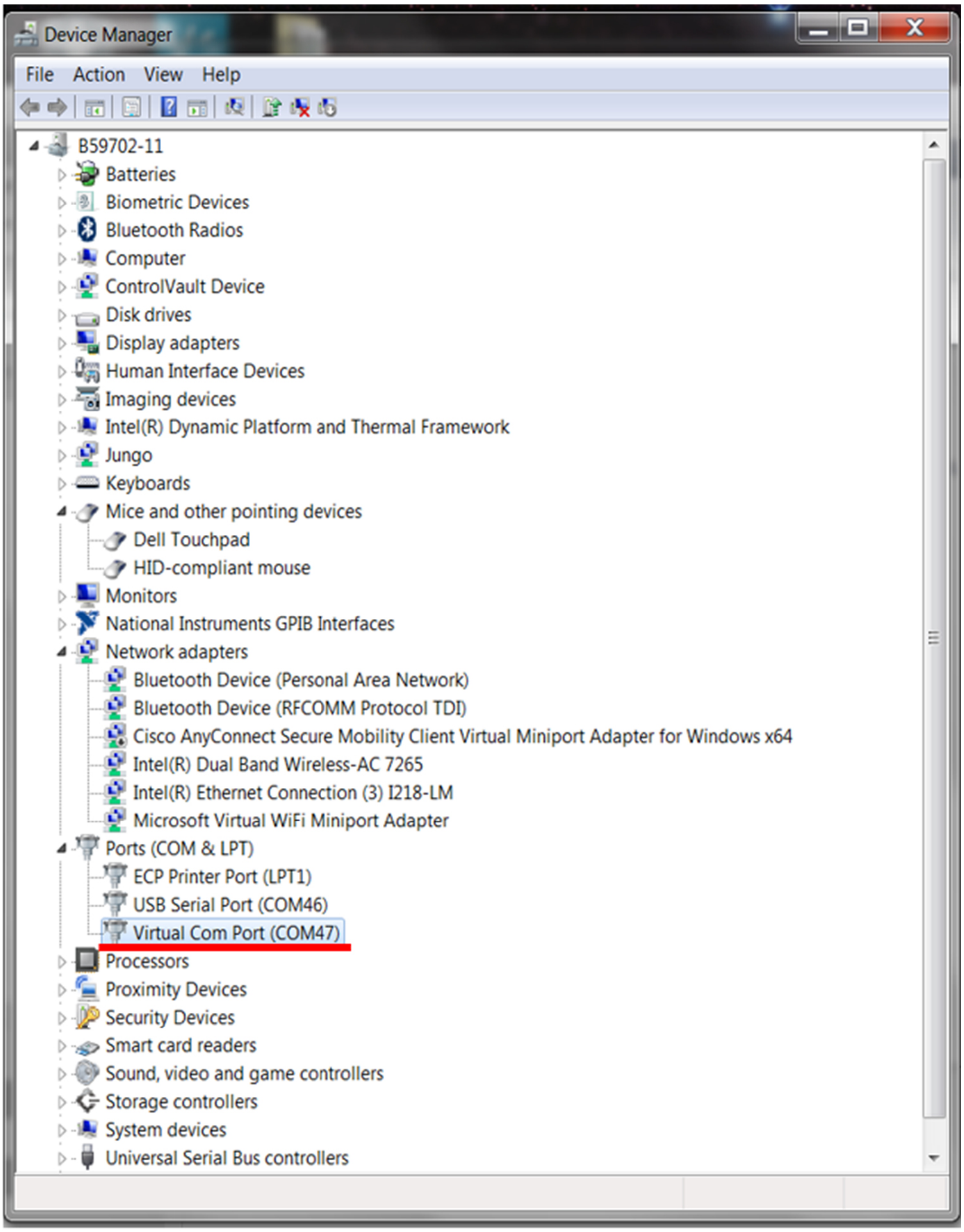
aaa-031992

14. In the **Virtual Com Port Properties** window, verify that the device is working properly, and then click **Close**.



aaa-031993

The Virtual Com Port appears in the Device Manager window.



aaa-031994

5.3 Installing FlexGUI software package

The FlexGUI software installation requires only extracting the zip file in a desired location.

1. If necessary, install the Java JRE and Windows 7 FlexGUI driver.
2. Download the latest FlexGUI (32-bit or 64-bit) version, available at http://www.nxp.com/KITVR55-FSSKTEVM.
3. Run the flexgui-app-vr5500-fs5502.exe, install the FlexGUI with step by step guidance.

6 Configuring the hardware for startup

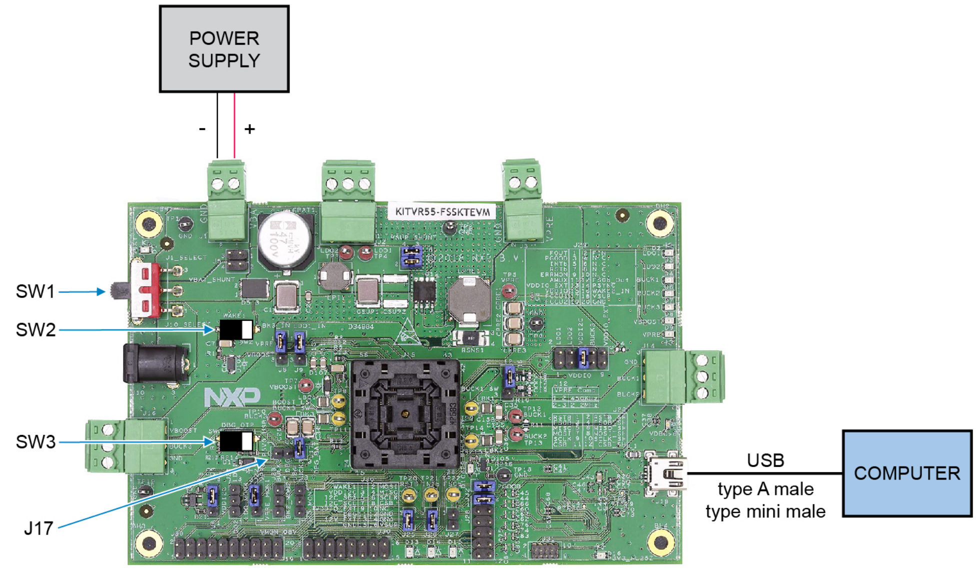


Figure 16. Typical initial configuration

Figure 16 presents a typical hardware configuration incorporating the development board, power supply, and Windows PC workstation.

To configure the hardware and workstation as illustrated in Figure 16, complete the following procedure:

1. Install jumpers for the configuration.

Table 16. Jumper configuration

Jumper	Configuration
J17	connect 1-2 (connect 5.0 V on DBG pin from the USB)

2. Configure switches for the configuration

Table 17. Switch configuration

Switch	Configuration
SW1	middle position (VBAT off)
SW2	open (WAKE1)
SW3	open (OTP programming off)

3. Connect the Windows PC USB port to the KITVR55-FSSKTEVM development board using the provided USB 2.0 cable.
   Set the DC power supply to 12 V and current limit to 1.0 A. With power turned off, attach the DC power supply positive and negative output to KITVR55-FSSKTEVM V_{BAT} Phoenix connector (J1).
4. Turn on the power supply.
5. Close SW2.

Note: *At this step, the product is in debug mode and all regulators are turned off. The user can then power up with OTP configuration or configure the mirror registers before power up. Power up is effective as soon as J17 jumper is removed.*

7 Using the KITVR55-FSSKTEVM evaluation board

This section summarizes the overall setup. Detailed description is provided in the following sections.

Before starting the process, choose the mode you want to run the device.

- In Normal mode, the configuration comes from OTP fuses.
- In Debug mode, you can either use the current configuration from OTP fuse, if any, or use the OTP emulation mode to write in the mirror register.

The Normal mode or Debug mode is defined at startup depending on the DBG pin level.

- Normal mode is set by tying DBG to ground
- Debug mode is set by setting DBG voltage to 5.0 V

In OTP emulation, you can overwrite the mirror registers from a given OTP fuse configuration. See Section 4.2.1 and Section 8.3 to define your configuration.

In OTP fuse configuration, use the configuration fused in the OTP. So, if a valid OTP fuse configuration exists, then it is copied to the mirror registers at startup.

7.1 Generating the OTP configuration file

Define and generate your OTP configuration using the excel file *VR5500_OTP_Config.xlsm*. This file allows configuring the device for parameters controlled by the main state machine and the fail-safe state machine.

To generate the script:

1. Fill the **OTP_conf_main_reg** sheet

MAIN OTP_REGISTERS

Register Name	DDRES	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Data_Bin	Data_Hex
OTP_CFG_VPRE_1	14	-	-	VPREV[5:0]							
		0	0	001111 - 3.3V						00001111	0x0F
OTP_CFG_VPRE_2	15	-	-	VPRESC[5:0]							
		0	0	001110 - 140mV/us						00001110	0x0E
OTP_CFG_VPRE_3	16	VPREILIM[1:0]		VPRETOFF[1:0]		VPRESRLS[1:0]		VPRESRHS[1:0]			
		11 - 150mV		10 - 40ns		11 - PU/PD/900mA		00 - PU/PD/130mA		11101100	0xEC
OTP_CFG_BOOST_	17	otp_SPARE0[2:0]			Reserved	VBSTV[3:0]					
		000			0	1101 - 5.74V				00001101	0x0D
OTP_CFG_BOOST_	18	BOOSTEN	VBSTTONTIME[1:0]		VBSTSC[4:0]						
		1 - Enabled	00 - 60ns		01110 - 79mV/us					10001110	0x8E
OTP_CFG_BOOST_	19	VBSTRCOMP[1:0]		VBSTCCOMP[1:0]		VBSTILIM[1:0]		VBSTSR[1:0]			
		00 - 750kohms		00 - 125pF		01 - 2A		11 - 500V/us		00000111	0x07
OTP_CFG_BUCK1_	1A	VB1V[7:0]									
		10001000 - 1.25V								10001000	0x88
OTP_CFG_BUCK1_	1B	-	-	-	VB1INDOPT[1:0]		VB1SWILIM[1:0]		VB12MULTIPH		
		0	0	0	00 - 1uH		11 - 4.5A		0 - Disabled	00000110	0x06
OTP_CFG_BUCK2_	1C	VB2V[7:0]									
		10110001 - 1.8V								10110001	0xB1
OTP_CFG_BUCK2_	1D	-	VB2INDOPT[1:0]		BUCK2EN	VB2SWILIM[1:0]		VB3_CTRL_RC	VB3_CTRL_GM		
		0	00 - 1uH		1 - Enabled	01 - 2.6A		0 - Default	0 - Default	00010100	0x14
OTP_CFG_BUCK3_	1E	BUCK3EN	VB3INDOPT[1:0]		VB3V[4:0]						
		1 - Enabled	00 - 1uH		01110 - 2.3V					10001110	0x8E
OTP_CFG_BUCK3_	1F	VB2GMCOMP[2:0]			VB1GMCOMP[2:0]			VB3SWILIM[1:0]			
		010 - 32.5 GM			100 - 65 GM			11 - 4.5A		01010011	0x53
OTP_CFG_LDO	20	LDO2ILIM	LDO2V[2:0]			LDO1ILIM	LDO1V[2:0]				
		0 - 400mA	111 - 5.0V			0 - 400mA	110 - 3.3V			01110110	0x76
OTP_CFG_SEQ_1	21	-	-	VB2S[2:0]			VB1S[2:0]				
		0	0	001 - Regulator Start and Stop in Slot 1			010 - Regulator Start and Stop in Slot 2			00001010	0x0A
OTP_CFG_SEQ_2	22	-	-	LDO2S[2:0]			LDO1S[2:0]				
		0	0	111 - Regulator Does not Start (Enabled by SPI)			011 - Regulator Start and Stop in Slot 3			00111011	0x3B
OTP_CFG_SEQ_3	23	otp_SPARE1[4:0]					VB3S[2:0]				
		00000					000 - Regulator Start and Stop in Slot 0			00000000	0x00
OTP_CFG_CLOCK_	24	-	-	VPRE_ph[2:0]			CLK_DIV2[2:0]				
		0	0	000 - delay 0			100 - divide by 44 - CLK2=455KHz			00000100	0x04
OTP_CFG_CLOCK_	25	-	-	BUCK1_ph[2:0]			VBST_ph[2:0]				
		0	0	110 - delay 6			000 - no delay			00110000	0x30
OTP_CFG_CLOCK_	26	-	-	BUCK3_ph[2:0]			BUCK2_ph[2:0]				
		0	0	000 - no delay			011 - delay 3			00000011	0x03
OTP_CFG_CLOCK_	27	BUCK3_clk_sel	BUCK2_clk_sel	BUCK1_clk_sel	VBST_clk_sel	VPRE_clk_sel	PLL_sel	CLK_DIV1[1:0]			
		0 - CLK1	0 - CLK1	0 - CLK1	0 - CLK1	1 - CLK2	0 - Disabled	10 - divide by 9 - CLK1=2.22MHz		00001010	0x0A
OTP_CFG_SM_1	28	-	-	conf_tsd[5:0]							
		0	0	0 - BOOST Shutdown	0 - BUCK1 Shutdown	0 - BUCK2 Shutdown	0 - BUCK3 Shutdown	0 - LDO1 Shutdown	0 - LDO2 Shutdown	00000000	0x00
OTP_CFG_SM_2	29	-	-	-	VPRE_off_dly	Autoretry_infinite	Autoretry_en	PSYNC_CFG	PSYNC_EN		
		0	0	0	0 - 250us	1 - Enabled	1 - Enabled	0 - 2x FS85	0 - Disabled	00001100	0x0C
OTP_CFG_VSUP_U	2A	otp_SPARE2[6:0]							VSUPCFG		
		0000000							0 - 4.9V for Vpre < 4.5V	00000000	0x00
OTP_CFG_I2C	2B	-	-	-	-	M_I2CDEVADDR[3:0]					
		0	0	0	0	0000 - Address D0				00000000	0x00
OTP_CFG_OV	2C	-	-	-	-	-	VDDIO_REG_ASSIGN[2:0]				
		0	0	0	0	0	001 - VPRE			00000001	0x01
OTP_CFG_DEVID	2D	DeviceID[7:0]									
		00000001								00000001	0x01
OTP_M_S1_CRC_LS	2E	OTP_M_S1_CRC_LSB[7:0]									
		Automatically filled in by Sidence IP								00000000	0x00
OTP_M_S1_CRC_MS	2F	OTP_M_S1_CRC_MSB[7:0]									
		Automatically filled in by Sidence IP								00000000	0x00

aaa-035261

Figure 17. OTP_conf_main_reg spreadsheet example

2. Fill the **OTP_conf_failsafe_reg** sheet

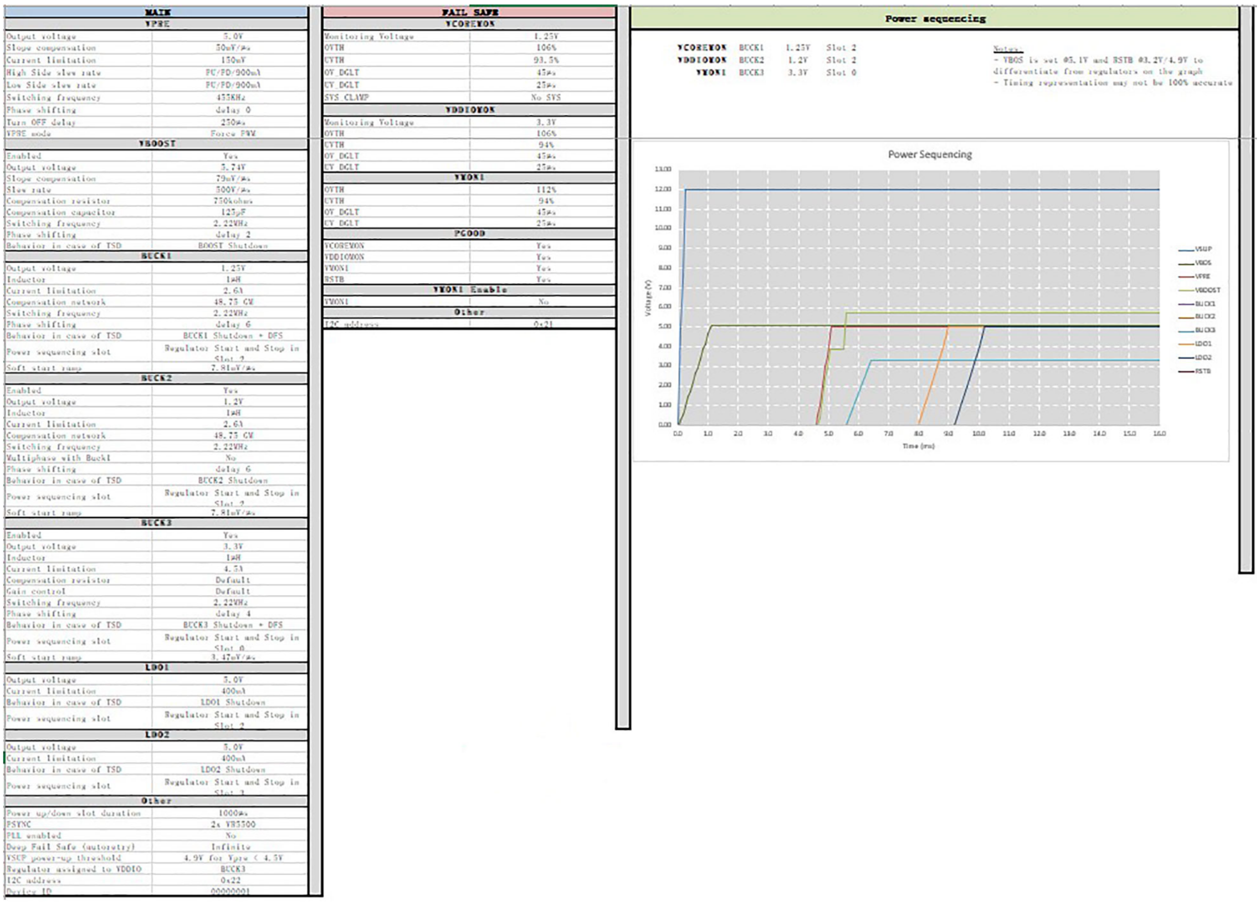
FAIL-SAFE OTP_REGISTERS

Register Name	ADDRESS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Data_Bin	Data_Hex
OTP CFG UVOV 1	0A	VCORE_V[7:0]									
		10001000 - 1.25V								10001000	0x88
OTP CFG UVOV 2	0B	VDDIOOVTH[3:0]				VCOREOVTH[3:0]					
		0011 - 106%				0011 - 106%				00110011	0x33
OTP CFG UVOV 3	0C	-	-	VDDIO_V	VCORE_SVS_CLAMP[4:0]						
		0	0	0 - 3.3V	00000 - No SVS					00000000	0x00
OTP CFG UVOV 4	0D	-	-	-	-	VMON1OVTH[3:0]					
		0	0	0	0	1111 - 112%				01111	0x0F
OTP CFG UVOV 5	0E	-	-	-	-	-	-	-	-		
		0	0	0	0	0	0	0	0	00	0x00
OTP CFG UVOV 6	0F	VDDIOUVTH[3:0]				VCOREUVTH[3:0]					
		0011 - 94%				0100 - 93.5%				00110100	0x34
OTP CFG UVOV 7	10	-	-	-	-	VMON1UVTH[3:0]					
		0	0	0	0	0011 - 94%				00011	0x03
OTP CFG UVOV 8	11	-	-	-	-	-	-	-	-		
		0	0	0	0	0	0	0	0	00	0x00
OTP CFG PGOOD	12	-	PGOOD_RSTB	-	-	-	PGOOD_VMON1	PGOOD_VDDIO	PGOOD_VCORE		
		0	1 - Assigned	0	0	0	1 - Assigned	1 - Assigned	1 - Assigned	01000111	0x47
OTP CFG ABIST1	13	otp_SPARE0[1:0]		-	-	-	-	-	-		
		00		0	0	0	1	1	1	00000111	0x07
OTP CFG ASIL	14	-	-	-	-	-	-	-	VMON1_EN		
		1	0	0	0	0	0	0	0 - Disabled	10000000	0x80
OTP CFG I2C	15	otp_SPARE1[2:0]			-	FS_I2CDEVADDR[3:0]					
		000			0	0000 - Address D0				00000000	0x00
OTP CFG DGLT DUR 1	16	otp_SPARE2[1:0]		VCORE_UV_DGLT[1:0]		VCORE_OV_DGLT	VDDIO_UV_DGLT[1:0]		VDDIO_OV_DGLT		
		00		10 - 25µs		1 - 45µs	10 - 25µs		1 - 45µs	00101101	0x2D
OTP CFG DGLT DUR 2	17	otp_SPARE3[4:0]					VMON1_UV_DGLT[1:0]		VMON1_OV_DGLT		
		00000					10 - 25µs		1 - 45µs	00000101	0x05
OTP FS S1 CRC LSB	18	OTP_FS_S1_CRC_LSB[7:0]									
		Automatically filled in by Sidence IP								00000000	0x00
OTP FS S1 CRC MSB	19	OTP_FS_S1_CRC_MSB[7:0]									
		Automatically filled in by Sidence IP								00000000	0x00

aaa-035262

Figure 18. OTP_conf_failsafe_reg spreadsheet example

3. See the **OTP_conf_summary** sheet to review the complete configuration (main and fail-safe)



aaa-035263

Figure 19. OTP_conf_summary example

4. Generate the script in **OTP_conf_file_generation** sheet
   Once the configuration is ready, the user can generate the script file. Go to **OTP_conf_file_generation**, enter the path in the **File repository**, and then click **Write_OTP_File_GUI**.

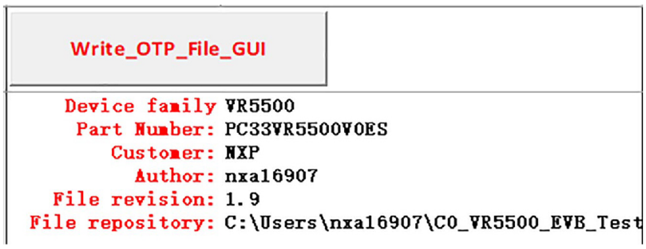


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Figure 20. OTP script generation

7.2 Working in OTP emulation mode

At startup, the device always uses the content from the mirror register. This content can come from OTP fuse or from configuration written directly in the mirror register. OTP emulation means that the user can emulate the OTP writing in the mirror register. It allows trials before burning the OTP.

1. Configure the hardware; see Section 6.
2. Launch the FlexGUI software.
3. Switch to Debug mode:
   a. Place SW1 in TOP direction (V_{BAT} switched on).
   b. Close SW2 (WAKE1).
   While in Debug mode, all regulators are turned off.
4. Load the mirror registers to work in OTP emulation mode; see Section 8.3.
5. Unplug jumper J17 1-2 to start the device with the mirror configuration setting.
   a. If the mirror registers are filled (with a configuration using the Script editor), that configuration is used in the emulation session.
   b. If the mirror registers are not filled (with a configuration using the Script editor), the currently programmed OTP fuse configuration is used, if it exists.
   c. Otherwise, the mirror registers are not filled and the OTP fuse is not burned, and the device does not start up.
6. Use the FlexGUI software to evaluate the device configured; see Section 8.

7.3 Programming the device with an OTP configuration

The device configuration can be changed three times (see Section 4.2.1). The programming steps are the same as the OTP emulation mode up to step 6.

Then, the user has to burn the part with FlexGUI; see Section 8.4.7. Follow the instructions on the screen to proceed.

8 Using FlexGUI

To follow the steps in this section, make sure that the board is connected using the appropriate hardware configuration (see Section 7.2).

Note: *It is recommended to use the latest version of FlexGUI.*

8.1 Starting the FlexGUI application

After launching the FlexGUI, the FlexGUI launcher displays available kits.

Select I^2C-bus as communication bus on the launcher page.

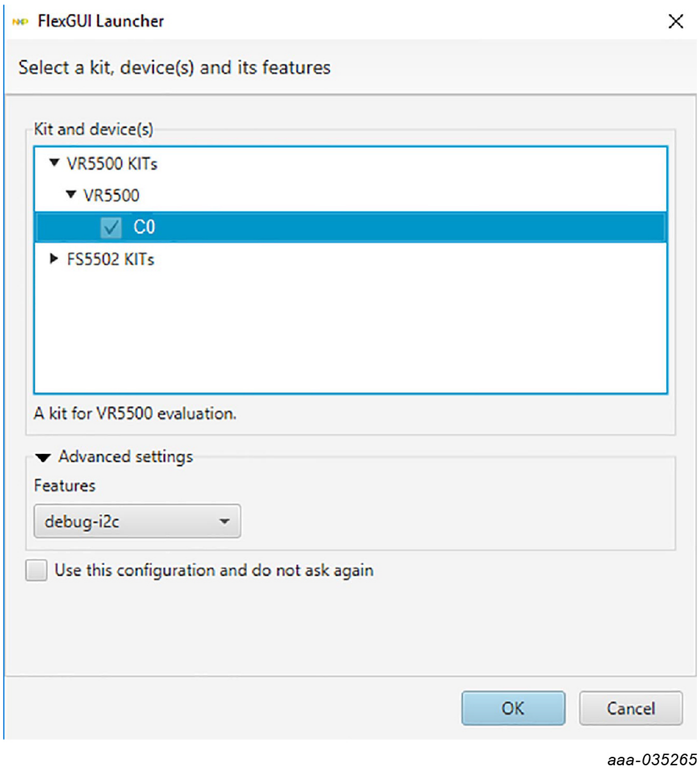


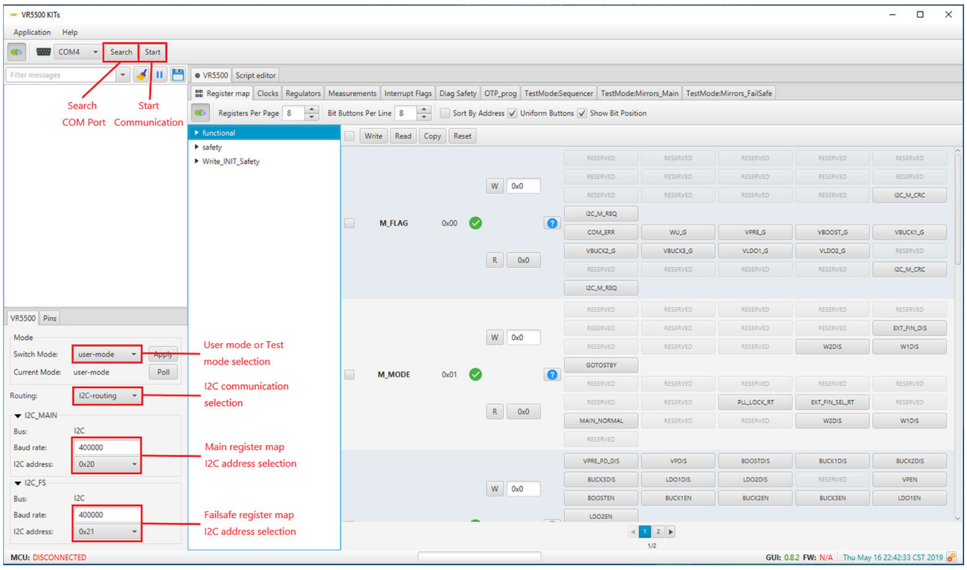
Figure 21. Launcher panel - bus selection

When the configuration is selected, click **OK**.

8.2 Establishing the connection between FlexGUI and the hardware

The board must be connected to the USB before establishing a connection.

- Click **Search** to detect the COM port of the board.
- Click **Start** to enable the connection.



aaa-035266

Figure 22. Main panel

Figure 22 shows the mode selection. At first launch, the FlexGUI starts in User mode. The user can then decide to switch to Test mode using the Switch mode drop-down list followed by clicking **Apply**.

The **GUI-Device Status** field checks the connection from MCU to the device. The **ONLINE** status indicates a good connection, while **ERROR** status indicates an issue (for example V_{SUP} is not provided to the device).

Select I^2C-bus as communication bus.

It is also possible to change the clock frequency using this panel.

Note that in the case of I^2C-bus, most of the time, the default address used by the device are 0x20 for main and 0x21 for the fail-safe.

The I^2C-bus address is managed differently in Debug and Normal mode

- Debug mode:
  - I^2C-bus address when debug mode pin is set to 5.0 V is 0x20 for main and 0x21 for fail-safe.
  - The user can change this address in the mirror register. The new address is taken into account only after debug pin is released to 0 V.
- Normal mode:
  - The address is burned in the OTP.

The user can read in which mode the device is operating. It is also possible to switch from User mode to Test mode (and the opposite way).

The current operating mode is refreshed periodically by default at FlexGUI startup. This automatic refresh can be disabled by disabling Poll button as shown in Figure 23.

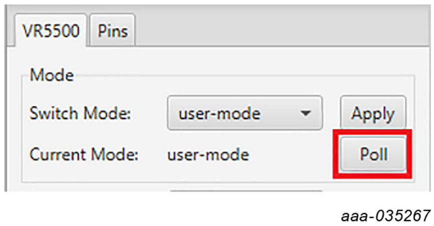


Figure 23. Disabling device mode polling

To move from one mode to the other, select the mode with switch mode drop-down button and click **Apply** to validate. Now, the current mode is updated at the condition that Poll button is enabled.

8.3 Working with the script editor

The register and OTP emulation can be configured with the script editor. It is useful to try various OTP configurations in Emulation mode.

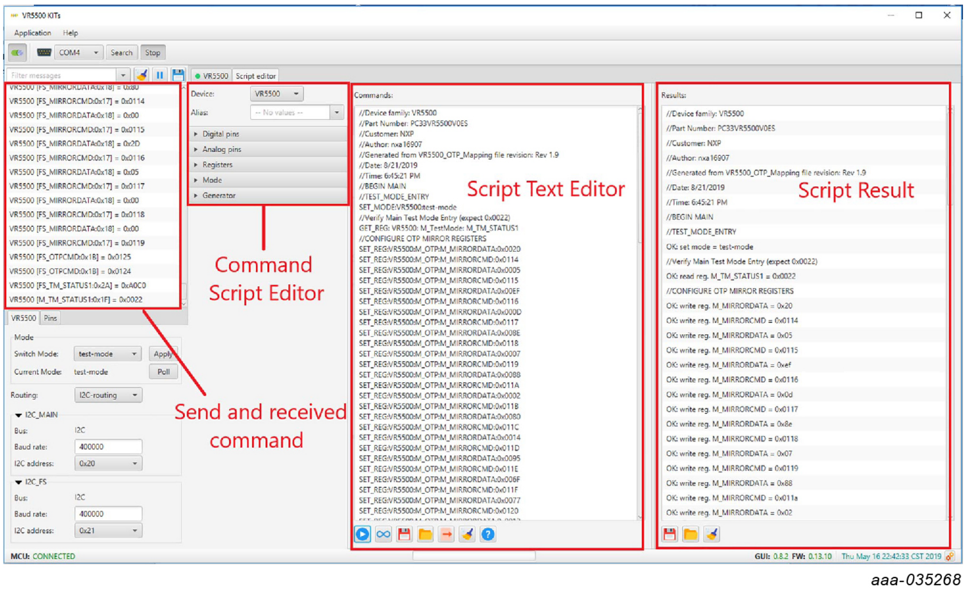


Figure 24. Script editor

The main subareas of this panel are:

- **Send and receive command**: displays a summary of commands sent and received from the device
- **Command script editor**: builds commands to be sent to the device
- **Script text editor**: sends a sequence of register configurations from a text file or from command edited directly in this area
- **Script results**: displays result status of each command sent to the device

8.3.1 Script text editor

Using script editor, you can execute any command either directly or from a file. It is also possible to save and modify a script. Using the brush symbol, it is possible to clean windows if needed.

All commands have to follow a specific syntax. The Help menu describes commands available in the script editor and their syntax.

This help page describes commands available in the script editor and their format.

List of commands

- **SET_REG**: sets value of a selected register.
- **READ_REG**: reads value of a selected register.
- **SET_DPIN**: sets value of a selected digital pin.
- **GET_DPIN**: gets value of a selected digital pin.
- **GET_APIN**: gets value of a selected analog pin. Returned value is in mV.
- **PAUSE**: shows a dialog with user defined message. The script is paused until the user cofirms the dialog.
- **EXIT**: stops execution of the script.
- **SET_MODE**: sets device mode. List of modes depends on a device.

Command format

The following table describes command parameters. All paramaters are mandatory.

	1st parameter	2nd parameter	3rd parameter	4th parameter	5th parameter
SET_REG	Device	Reg. set	Reg. name / Reg. address	Reg. value	-
GET_REG	Device	Reg. set	Reg. name / Reg. address	-	-
SET_DPIN	Device	Pin name	Dig. pin value	-	-
GET_DPIN	Device	Pin name	-	-	-
GET_APIN	Device	Pin name	-	-	-
PAUSE	Message	-	-	-	-
EXIT	-	-	-	-	-

Description of command parameters mentioned in the table above:

- **Device**: device name (alias used in application).
- **Reg. set**: register set name. Register sets allows to associate registers which have similar function.
- **Reg. name**: register name as defined in datasheet.
- **Reg. address**: register address in decimal or hexadecimal (with 0x prefix) format.
- **Reg. value**: register value in decimal or hexadecimal (with 0x prefix) format.
- **Pin name**: name of digital or analog pin as defined in device datasheet.
- **Dig. pin value**: value of digital pin. Allowed strings are 'low' and 'high'.
- **Message**: a message to be displayed in a dialog. It cannot contain ':' character, which is used as delimiter of parameters.
- **Mode**: name of a device mode.

Figure 25 shows an example to build a command from the panel.

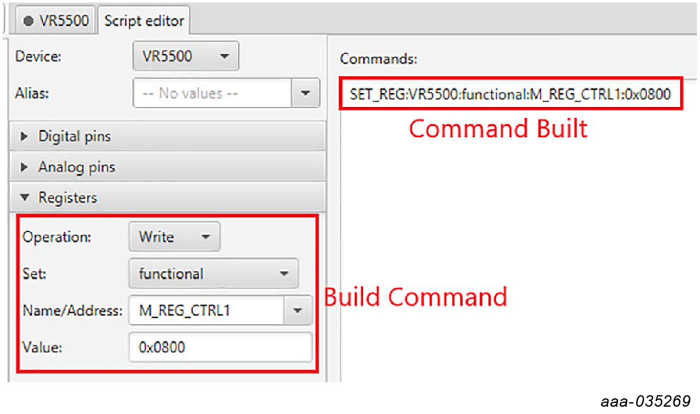


Figure 25. Build a command

The value 0x0800 is sent to the register M_REG_CTRL1 (BUCK2DIS). The user can then send it to the device by clicking the arrow; see Figure 26.

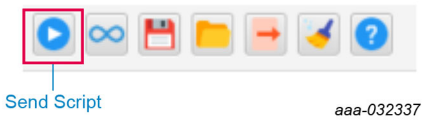


Figure 26. Send script

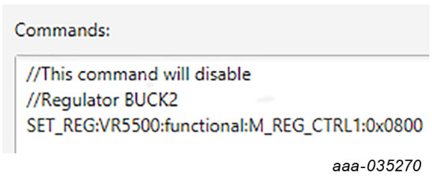


Figure 27. Correct format

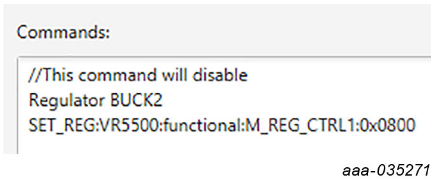


Figure 28. Wrong format ("//" missing in second line)

8.4 Understanding the VR5500 workspace

The VR5500 workspace consists of several tabs, each dedicated to a specific aspect of device functionality or configuration.

- Register map
- Clocks
- Regulators
- Measurements
- Interrupt flags
- Diag safety
- OTP programming
- TestMode:Sequencer
- TestMode:Mirrors_Main and TestMode:Mirrors_FailSafe

8.4.1 Register map

All I²C-bus registers can be accessed in write and read mode using this tab.

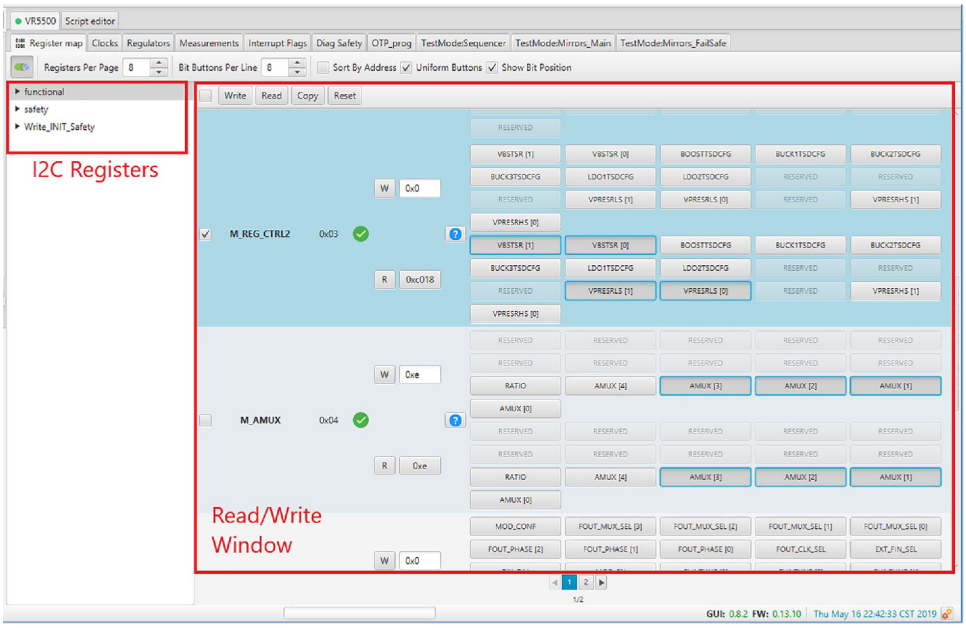


Figure 29. Register map

- **Register map**: allows access to functional register, safety register, and write init register which are accessible only during initialization phase
- **Read/write**: allows you to read/write any register either individually or by bank

8.4.2 Clocks

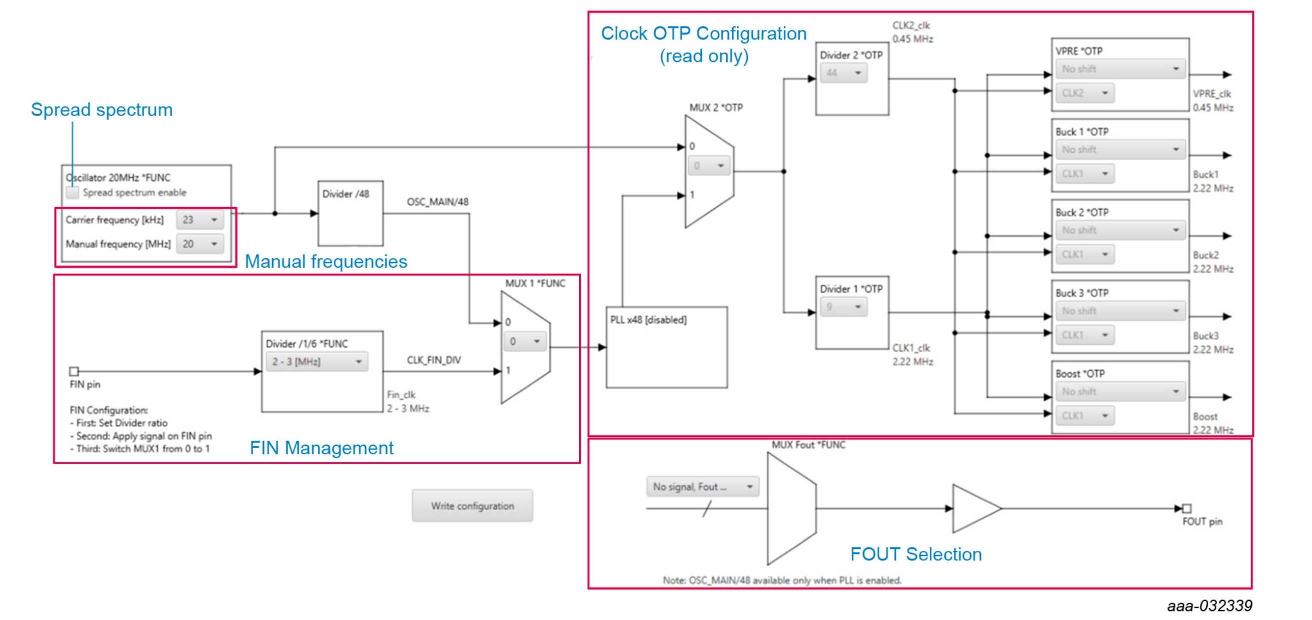


Figure 30. Clocks

This tab allows:

OTP:

- Read current OTP configuration (write operation is not possible). To display the accurate data, the device must operate in Test mode.

I^2C-bus:

- Configure the device to work with FIN input
- Select the signal to apply on FOUT pin
- Play with manual frequencies and spread spectrum

8.4.3 Regulators

The regulator has two main areas:

- Low voltage (LV) regulators configuration
- VPRE compensation network calculation

Each regulator can either be enabled or disabled by I2C. The thermal shutdown behavior can be configured to either shutdown the regulator, or shutdown the regulator and transition to deep fail-safe. The write button applies to the entire table. The VPRE compensation network calculator helps to define the value for VPRE external compensation network.

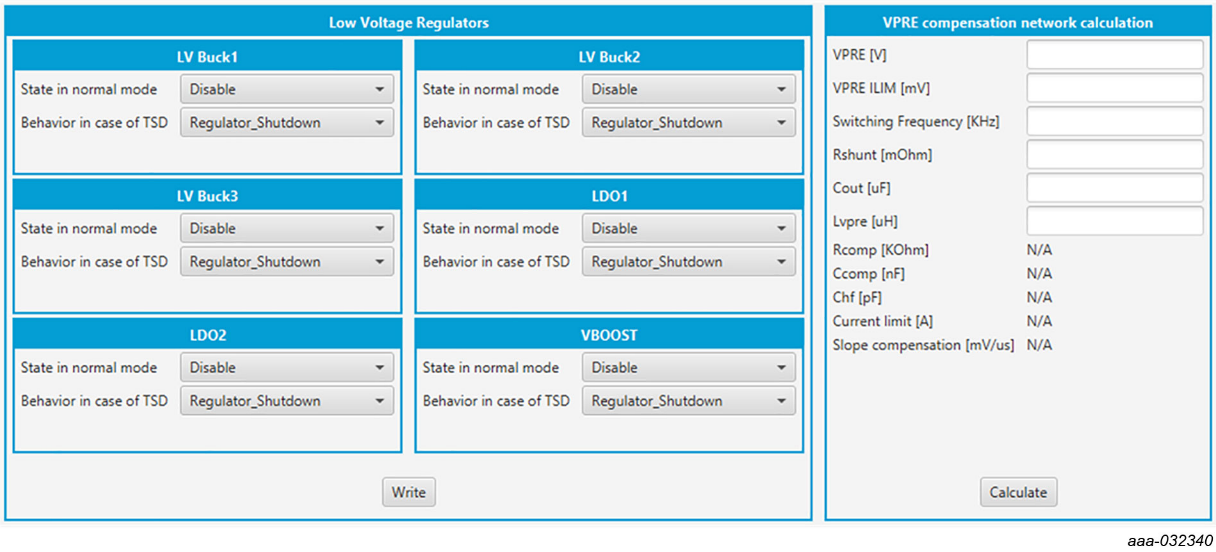


Figure 31. Regulators

8.4.4 Measurements

This tab enables two features:

- Read any of the AMUX signals over time
- Display regulator voltage summary

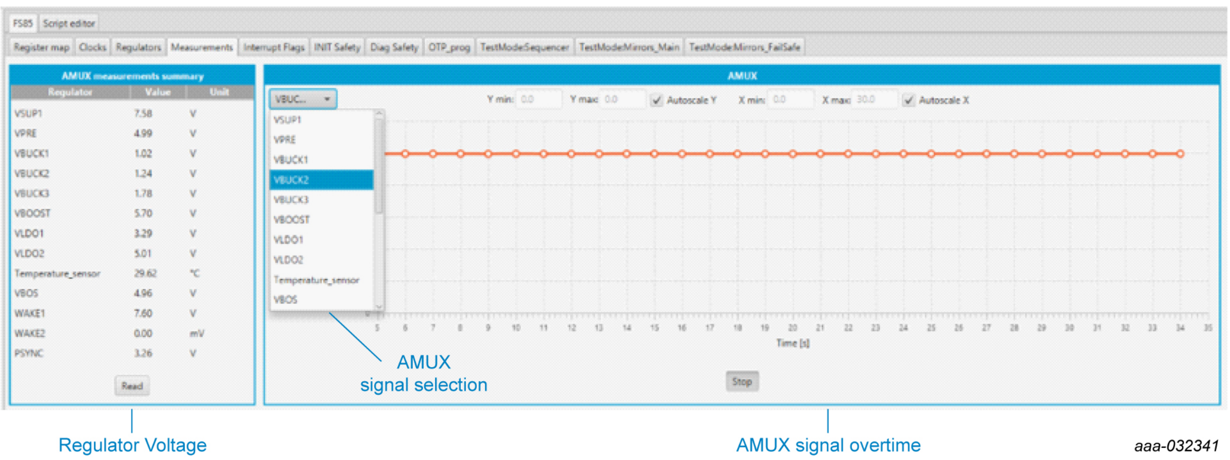


Figure 32. Measurements

8.4.5 Interrupt flags

This tab allows you to set or clear flags. It is also possible to mask the interruption.

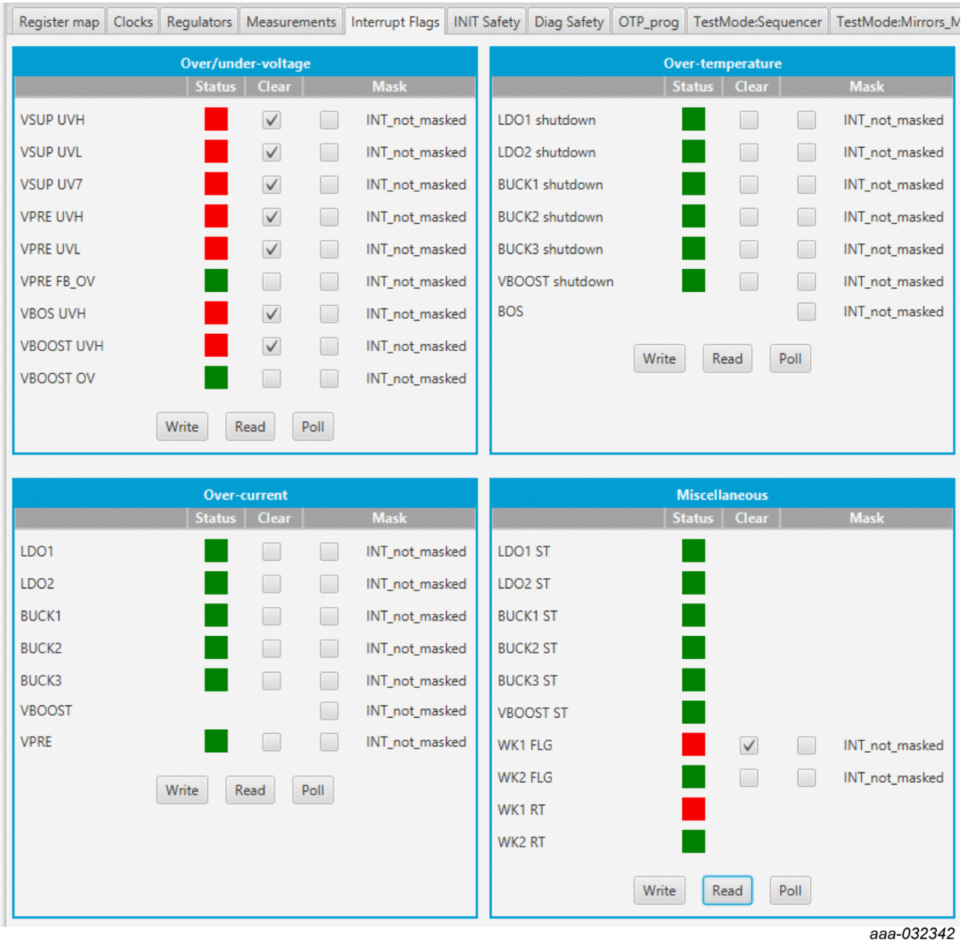


Figure 33. Interrupt flags

8.4.6 Diag safety

This tab shows the safety-related status and flags.

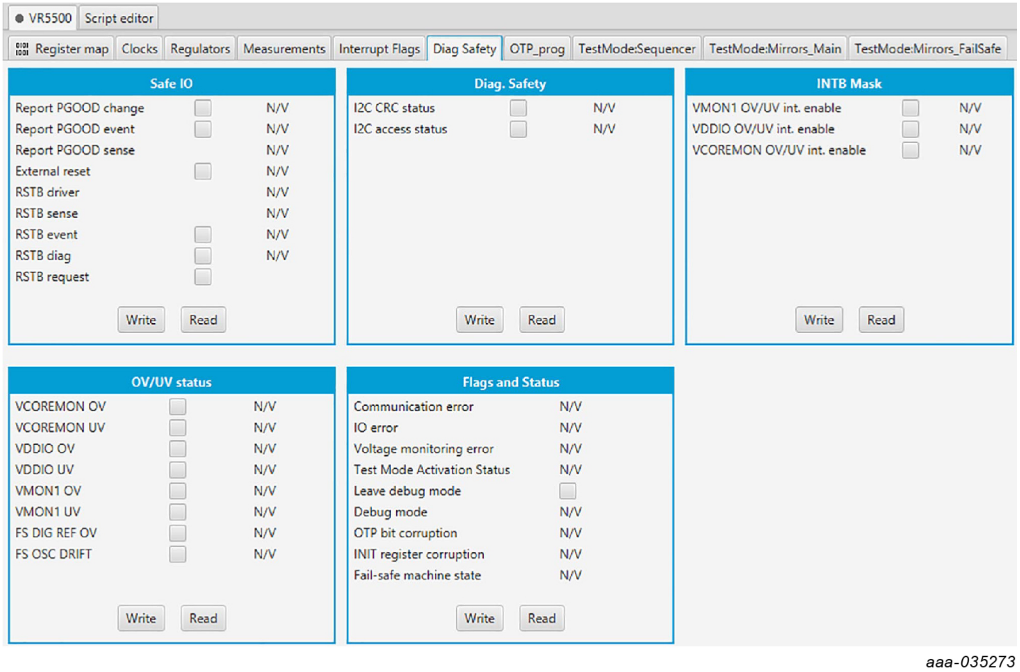


Figure 34. Diag safety

8.4.7 OTP programming

This tab allows you to burn the OTP using a script generated by the excel file OTP configuration; see Section 7.1.

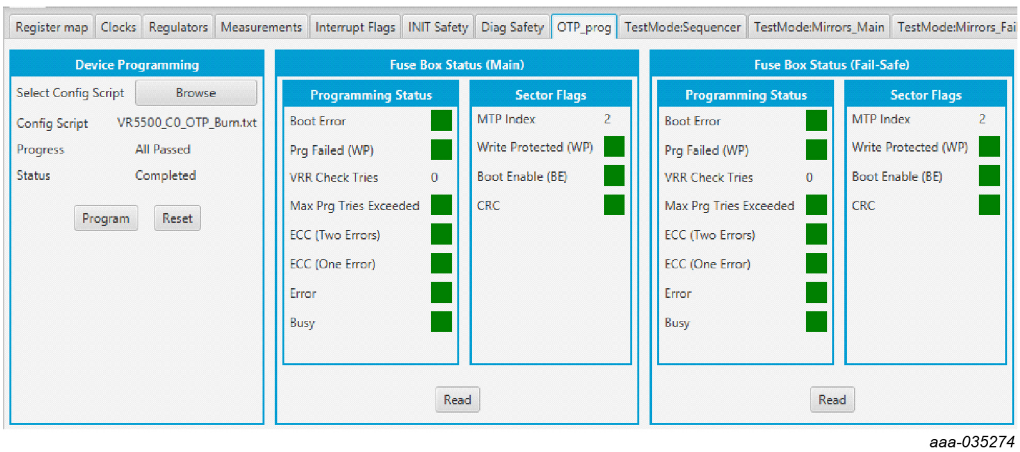


Figure 35. OTP burning

To set up the hardware before OTP burning, see Section 7.3.

See Figure 35 and follow the steps:

- Browse and load the script file you want to burn. The program button is then available.
- Click **Program**.

FlexGUI pops up to turn on the 8.0 V, and then turns off. The blue LED on the board indicates that an 8.0 V voltage is available on the debug pin. This voltage is used only during the burning process, and should not be applied in any other configuration. At the end of the first OTP programming, the MTP index = 1, WP, BE, and CRC flags are green.

The sector flags area status, Table 18 provides the state of main flags after a read. It helps to determine how many times the part was burned.

Table 18. OTP burning flag status

OTP burning step	BE	WP	CRC	MTP index
OTP is not burned; mirrors empty	red	red	red	1
OTP is not burned; mirrors filled	red	red	green	1
1	green	green	green	1
2	green	green	green	2
3	green	green	green	3

Example shown in Figure 35 corresponds to the OTP burning step 2 from Table 18.

To check if a valid OTP configuration is already burned, switch off V_{BAT}, then on, and start the device. The device starts with the OTP configuration.

8.4.8 TestMode:Sequencer

The sequencer allows you to display the slot configuration for the device. To be able to access this tab, the device has to be in Test mode. The configuration is read from mirror register. It is possible to modify it and update the mirror register.

As an example, the slot sequence is filled at startup with the content of OTP fuses. Then the user can decide to modify any of the configurations coming from the OTP fuse. All these actions are done with debug pin at 5.0 V and in Test mode.

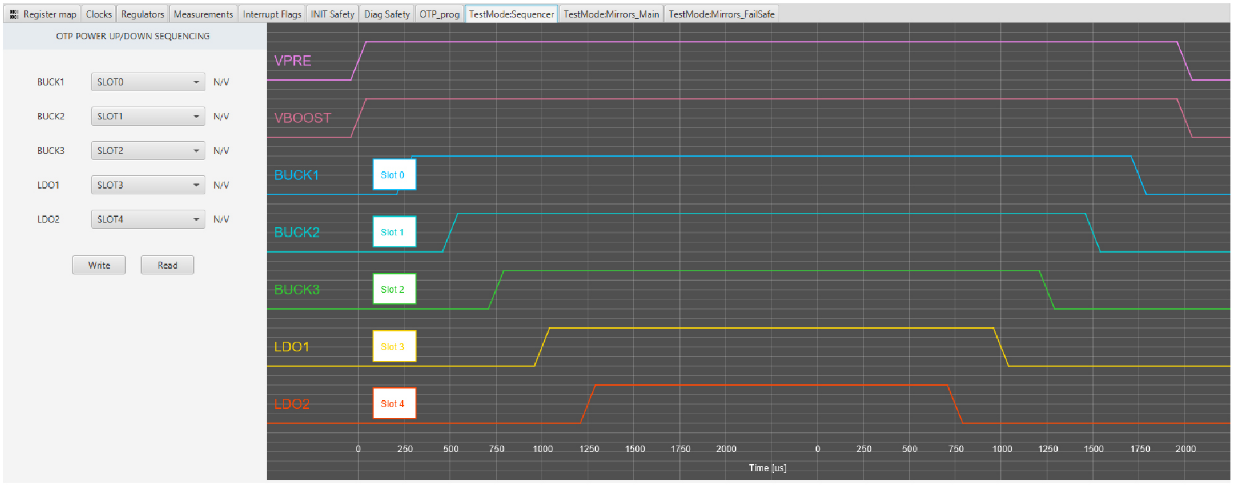


Figure 36. TestMode:Sequencer

Use the drop-down button (see Figure 37) to select the appropriate slot. The selection configuration can be sent to the device by clicking Write button. The current status can be read by using Read button.

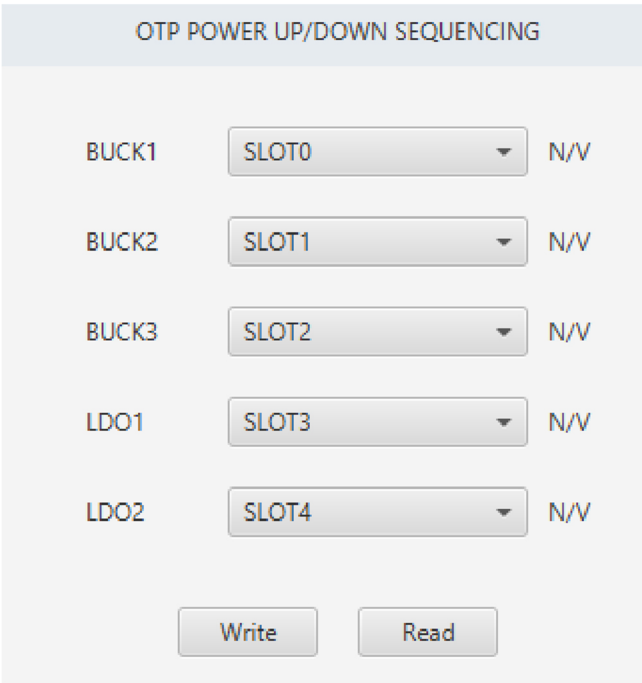
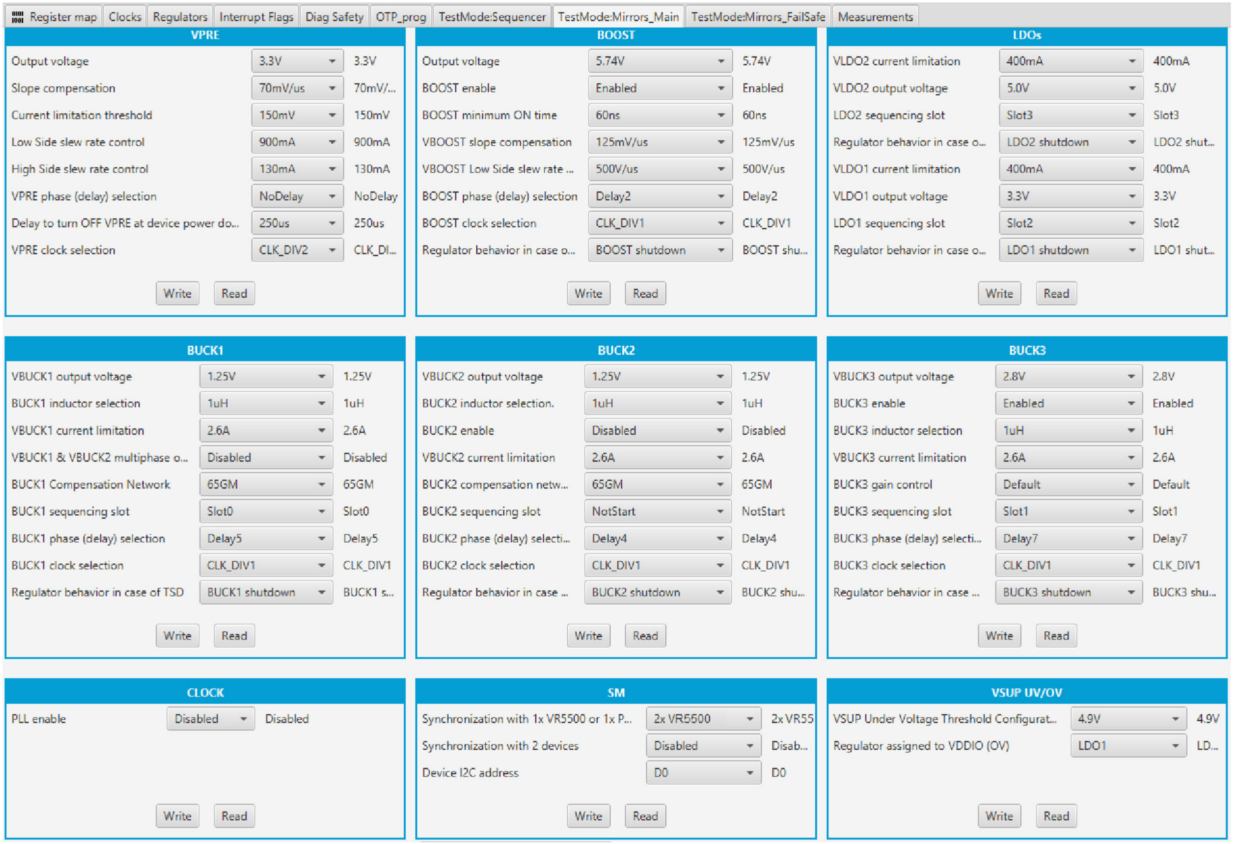


Figure 37. Slot management

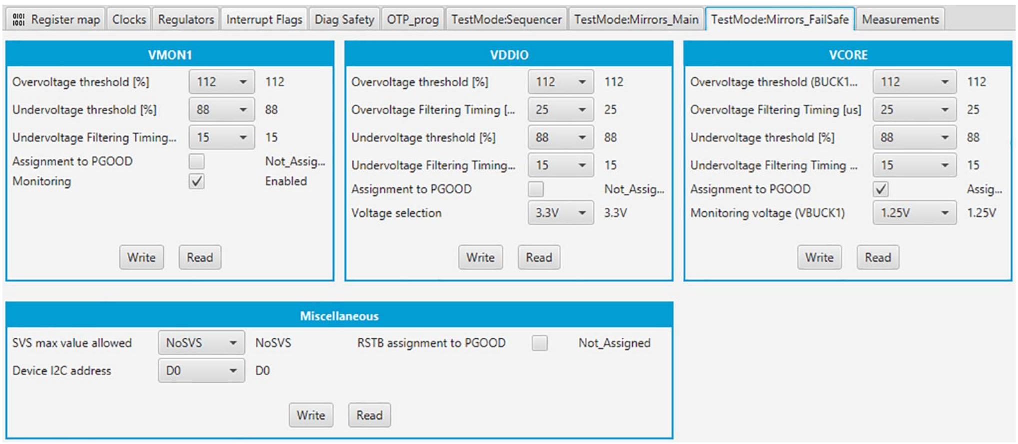
8.4.9 TestMode:Mirrors_Main and TestMode:Mirrors_FailSafe

The TestMode:Mirrors_Main and TestMode:Mirrors_FailSafe tabs allow access to the OTP main mirrors and fail-safe registers. These tabs are available in Test mode.



aaa-035484

Figure 38. TestMode:Mirrors_Main



aaa-035677

Figure 39. TestMode:Mirrors_FailSafe

The Read button provides the current status. The Write button changes the configuration in mirror register. It can be useful, for example, to modify few parameters from OTP fuse to start up the board.

9 References

[1] **KITVR55-FSSKTEVM** — detailed information on this board, including documentation, downloads, software and tools http://www.nxp.com/KITVR55-FSSKTEVM

[2] **VR5500** — product information on VR5500, high voltage PMIC with multiple SMPS and LDO http://www.nxp.com/VR5500

[3] **VR5500_OTP_Config.xlsm** — OTP configuration file

10 Revision history

Revision history

Rev	Date	Description
v.1	20191104	initial version

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Tables

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