UM11670

KITFS86SKTFRDMEM evaluation board

Rev. 1 — 5 November 2021 **User manual**

Document information

Information	Content
Keywords	FS8600, KITFS86SKTFRDMEM, KL25Z, I2C
Abstract	The KITFS86SKTFRDMEM provides flexibility to play with all the features of the device and make measurements on the main part of the application.

Revision history

Revision history

Rev	Date	Description
v.1	20211105	• Initial version

Important notice

NXP provides the enclosed product(s) under the following conditions:

This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The goods provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end product incorporating the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. In order to minimize risks associated with the customers applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact NXP sales and technical support services.

1 Introduction

The KITFS86SKTFRDMEM evaluation board user manual is intended for the engineers involved in the evaluation, design, implementation, and validation of FS8600 fail-safe system basis chips with multiple SMPS and LDOs.

The scope of this document is to provide the user with information to evaluate the FS8600 Fail-safe system basis chip with multiple SMPS and LDO.

The KITFS86SKTFRDMEM enables development on FS8600 family of devices. The kit can be connected to the NXP GUI software which allows you to play with registers, try OTP configurations, and burn the part.

The devices can be placed and removed easily from the board by using the socket. The device OTP can be burned twice, which provides a good flexibility. This board supports FS86 family of devices.

2 Finding kit resources and information on the NXP website

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on http://www.nxp.com.

The information page for KITFS86SKTFRDMEM evaluation board is at http://www.nxp.com/KITFS86SKTFRDMEM. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a Getting Started tab. The Getting Started tab provides quick-reference information applicable to using the KITFS86SKTFRDMEM evaluation board, including the downloadable assets referenced in this document.

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The NXP community is at https://community.nxp.com/.

3 Getting ready

Working with the KITFS86SKTFRDMEM requires the kit contents, additional hardware and a Windows PC workstation with installed software.

3.1 Kit contents

- Assembled and tested KITFS86SKTFRDMEM connected to a FRDM-KL25Z in an anti-static bag
- 3.0 ft USB-STD A to USB-B-mini cable
- Two connectors, terminal block plug, 2 pos., str. 3.81 mm
- Two connectors, terminal block plug, 3 pos., str. 3.81 mm
- Jumpers mounted on board
- Quick Start Guide

3.2 Additional hardware

In addition to the kit contents, the following hardware is necessary or beneficial when working with this kit.

- Power supply with a range of 8.0 V to 60 V and a current limit set initially to 1.0 A

3.3 Windows PC workstation

This evaluation board requires a Windows PC workstation. Meeting these minimum specifications should produce great results when working with this evaluation board.

- USB-enabled computer with Windows 7 or Windows 10

3.4 Software

Installing software is necessary to work with this evaluation board. All listed software is available on the evaluation board's information page at http://www.nxp.com/KITFS86SKTFRDMEM or from the provided link.

- NXP GUI for automotive PMIC families - latest version

4 Getting to know the hardware

The KITFS86SKTFRDMEM provides flexibility to play with all the features of the device and make measurements on the main part of the application. The KL25Z MCU Freedom board plugged on the board, combined with the NXP GUI software allows access to the registers in read and write mode. All regulators are accessible through connectors. Nonuser signal, like DC-DC switcher node is mapped on test points. Digital signals (I2C, RSTB, etc.) are accessible through connectors. Pin WAKE1 has a switch to control (Ignition) them. A VBAT switch is available to power On or Off the device.

The main purpose of this kit is to burn the OTP configuration. This kit can be operated in Emulation mode or in OTP mode. In Emulation mode, as long as the power is supplied, the board configuration stays valid, however the fail-safe configuration is lost if the device goes into deep fail-safe. The OTP mode uses the fused configuration. The device can be fused two times. In OTP mode, the device always starts with the fused configuration, except if the user wants to overwrite OTP configuration using Emulation mode. This board is able to fuse the OTP without any extra tools or board.

Note: *Due to the socket, this kit is not optimized for performance measurement or current higher than 1.0 A.*

4.1 Kit overview

The KITFS86SKTFRDMEM is a hardware evaluation tool that allows OTP burning. Due to the socket, the FS8600 part can be configured without the need to solder it. Devices can be programmed two times.

An Emulation mode is possible to test as many configurations as needed. An external LDO provides SUP_I2C voltage with a choice of 1.8 V or 3.3 V (default). From USB voltage, an external DC/DC generates the OTP programming voltage (8.0 V) without any need for an external power supply.

4.2 KITFS86SKTFRDMEM features

- VBAT power supply connectors (Jack and Phoenix)
- VPRE output capability up to 1.0 A (socket limit)
- VBUCK 1.0 V to 3.3 V
- VBOOST 5.0 V to 6.0 V
- LDO1 1.5 V to 5.0 V
- LDO2 1.1 V to 5.0 V
- Ignition key switch
- FS0B external safety pin
- Embedded USB connection for easy connection to software NXP GUI (access to I^2C-bus, IOs, RSTB, FS0B, INTB, Debug, MUX_OUT, regulators, register access, OTP emulation and programming)
- LEDs that indicate signals and regulator status
- Support OTP fuse capabilities
- Voltage monitoring jumper setting

4.3 Schematic, board layout and bill of materials

The schematic, board layout and bill of materials for the KITFS86SKTFRDMEM evaluation board are available at http://www.nxp.com/KITFS86SKTFRDMEM.

4.3.1 VMON board configuration

The VMONx configuration is highly dependent on the use case. This kit is delivered with a default configuration. However, the user can assign VMONx differently to address the use case using J26 connector and other parameters that will be detailed in this chapter. J26 can be seen in Figure 1.

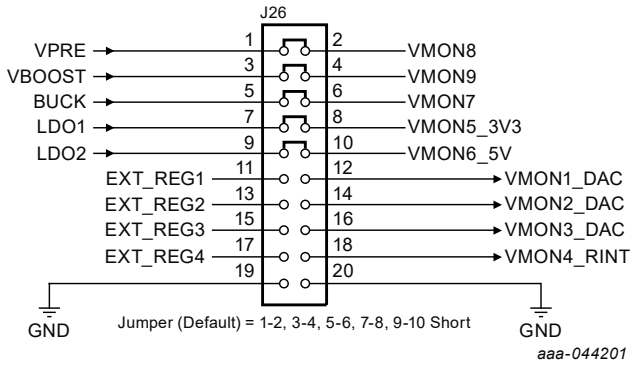

Figure 1. VMONx assignment

VMON1_DAC, VMON2_DAC, VMON3_DAC and VMON4_RINT use either DAC or internal resistor bridges (monitoring values are configurable by OTP for VMON4_RINT and VMONx_DAC). These VMONs are disconnected from any regulator by default but are still accessible through J26 connector.

By default, VMON5_RES and VMON6_RES pins are tied to a fixed 0.8 V supply (VMON_08V) using J18 and J20. This behaves like hardware disabling and makes debug easier. VMON5_RES and VMON6_RES can be tied to another regulator by changing the J18 and J20 configurations. In that case, these VMON use external fixed resistor bridges to adapt the VMON input voltage to 0.8 V. Resistors bridges values were

selected so that VMON5_RES and VMON6_RES would receive 0.8 V if VMONX_RES voltage inputs were respectively 3.3 V and 5.0 V. Figure 2 shows the corresponding part of the schematic.

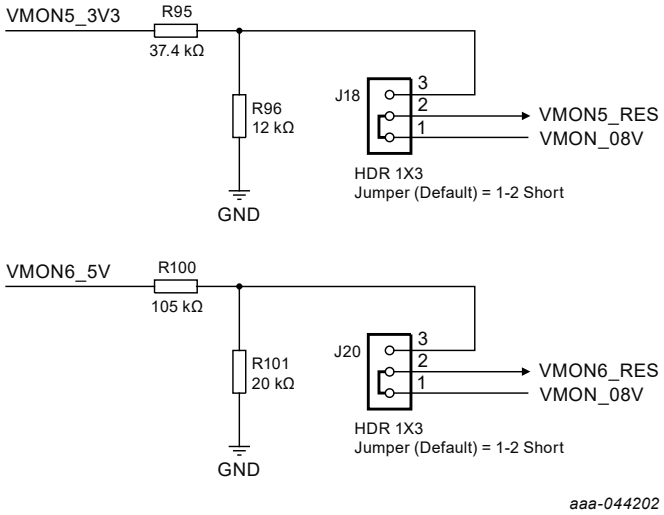

Figure 2. VMON5-6_RES input configuration

By default, VMON7_RES and VMON8_RES pins are tied, using respectively J17 and J19, to a fixed 0.8 V supply (VMON_08V). This behaves like hardware disabling and makes debug easy in some cases. VMON7_RES and VMON8_RES can be tied to another power supply by changing the J17 and J19 configuration. In that case, potentiometers are used to adapt the VMON input voltage to 0.8 V by adjusting the resistor bridge depending on the connected regulator nominal voltage.

By default, VMON9_RES uses a potentiometer to adapt the VMON input voltage to 0.8 V by adjusting the resistor bridge depending on the connected regulator nominal voltage.

Figure 3 shows the corresponding part of the schematic.

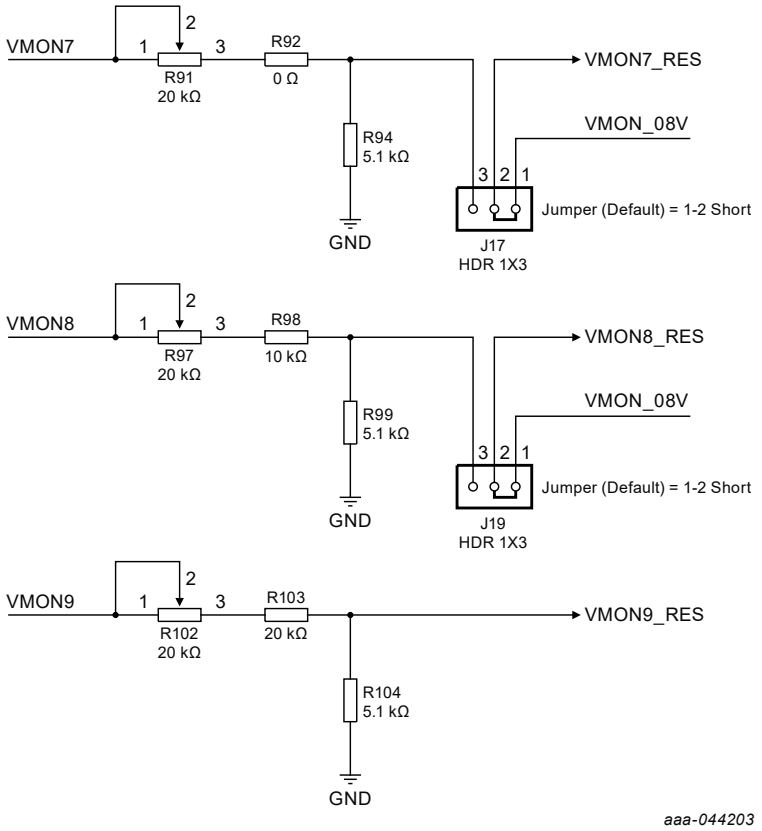

Figure 3. VMON7-8-9_RES input configuration

4.3.2 VPRE compensation network

This board is delivered with a VPRE compensation network defined for VPRE 4.1 V at 455 kHz. All other VPRE configurations (different voltage, output capacitors, inductor or current sense) require a new calculation for these components shown in Figure 4.

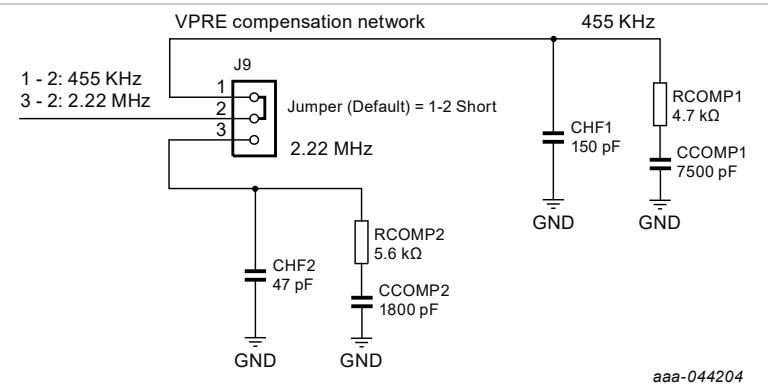

Figure 4. VPRE compensation network

Table 1 shows the recommendation for VPRE at both 455 kHz and VPRE 2.22 MHz.

Table 1. Compensation network

Components	VPRE 455 kHz	VPRE 2.22 MHz
CHF1/CHF2	150 pF	47 pF

Table 1. Compensation network*...continued*

Components	VPRE 455 kHz	VPRE 2.22 MHz
Ccomp1/Ccomp2	7.5 nF	1.8 nF
Rcomp1/Rcomp2	4.7 kΩ	5.6 kΩ
LPRE	From 4.7 µH to 10 µH	From 1.5 µH to 4.7 µH

4.3.3 Battery switch

The FS8600 has a battery switch function to disconnect the battery line from VPRE in case the external high side transistor is shorted. The battery switch functionality can be disabled by OTP. A PMOS is used to close the battery line at startup and open it in case of failure.

The transistor can be bypassed using J3 shown in Figure 5 if the function is not used.

Note: *The PMOS used has a maximum VDS voltage of 40 V. If the supply voltage is above this value, the PMOS must be bypassed.*

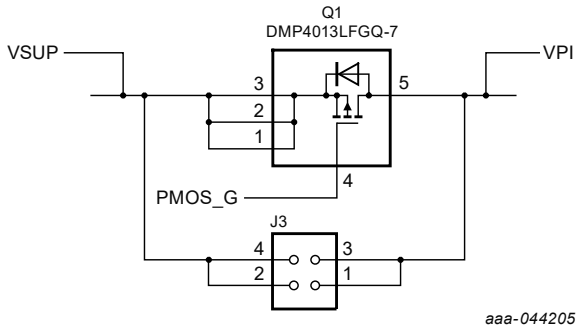

Figure 5. Battery switch

The PMOS gate is controlled by an external circuitry shown in Figure 7. An active solution using bipolar transistors is used to have better control performance. The objective is to have the fastest PMOS opening in case of VPRE HS failure.

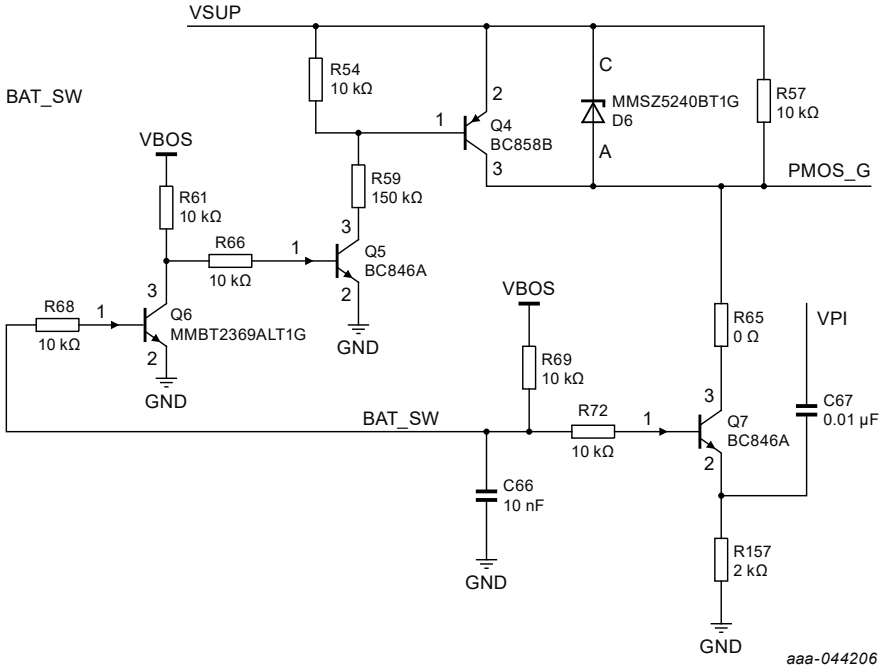

Figure 6. PMOS gate control circuitry

4.3.4 I²C

The I²C-bus is connected to KL25Z MCU to communicate with NXP GUI. However, if the user wants to connect the I²C to another MCU, this is possible. In this case, remove R133 and R132 to disconnect the KL25Z MCU (see Figure 7) and connect the external MCU on J25 connector as shown in Figure 8. In addition to this change, make sure that the VDDI2C voltage domain is the same on MCU side and SBC side.

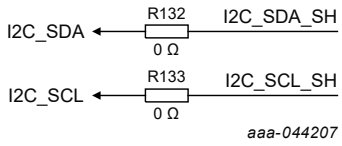

Figure 7. I²C connection to KL25Z

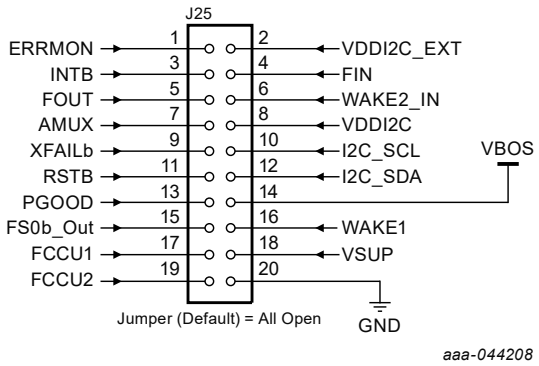

Figure 8. J25 I²C connection

4.3.5 VMON0_I2C

VMON0_I2C pin is powered through VDDI2C net and is used to supply internal buffers and I^2C communication. This supply is monitored through this pin depending on the OTP configuration. The monitoring voltage needs to be selected by the OTP.

The selection of VDDI2C is made using J13 connector as shown in Figure 9. As an option, an external LDO is provided to feed VDDI2C through the SUP_I2C net.

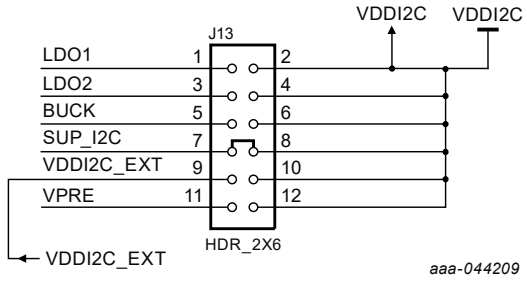

Figure 9. VDDI2C selection

The I^2C is compatible with 1.8 V or 3.3 V, therefore SUP_I2C voltage is configurable between 3.3 V or 1.8 V using J31 connector (3.3 V by default) shown in Figure 10.

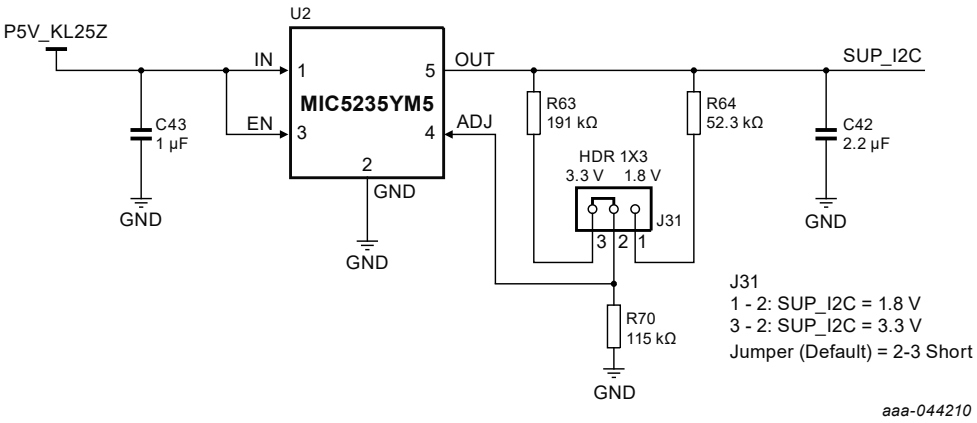

Figure 10. SUP_I2C supply

4.3.6 FIN external oscillator

In order to ease the FIN evaluation, a standalone oscillator is installed on the board. It supplies either 425 kHz or 2.4 MHz to the FIN input. The configuration is made using using J27 connector. Hardware implementation is shown in Figure 11.

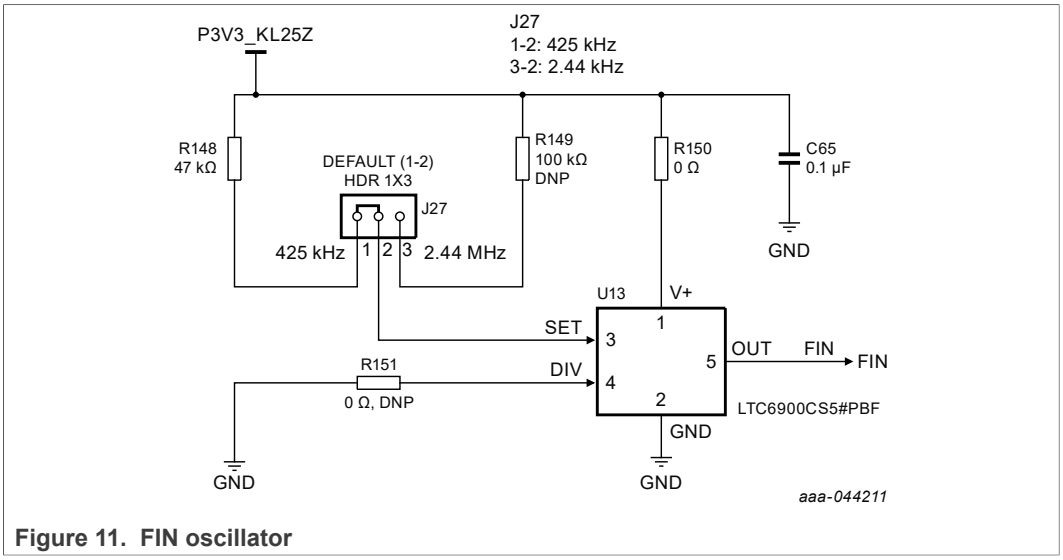

Figure 11. FIN oscillator

4.4 Kit featured components

Figure 12 identifies important components on the board and Table 2 provides additional details on these components.

Figure 12. Evaluation board featured components location

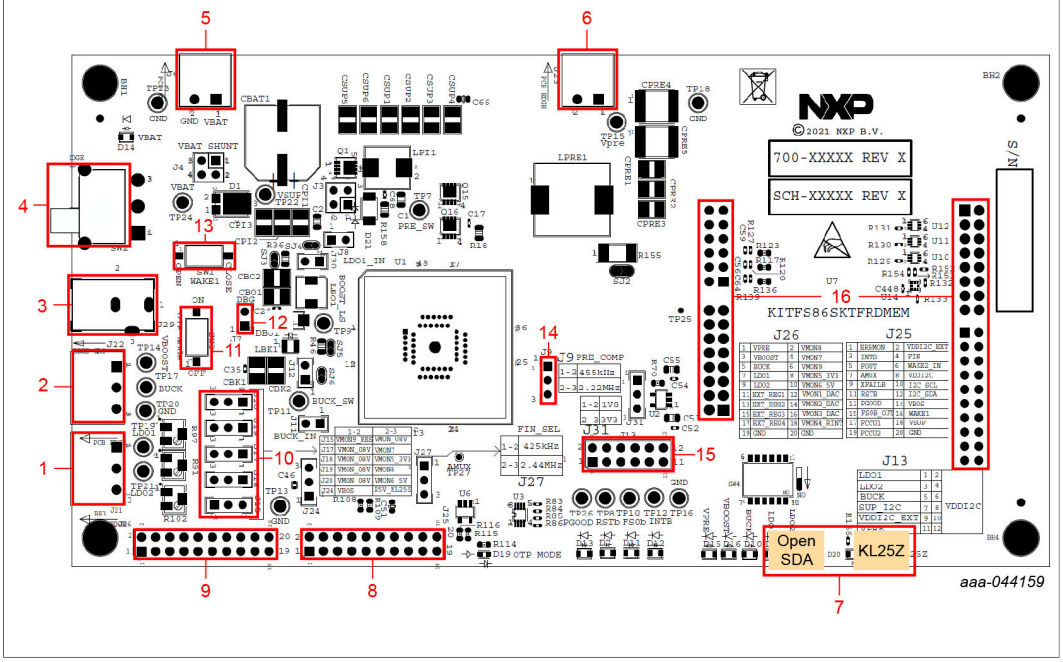

Table 2. Evaluation board featured components location

Number	Description
1	LDO1/LDO2 power supply
2	BUCK/BOOST power supply
3	VBAT Jack connector

Table 2. Evaluation board featured components location...*continued*

Number	Description
4	VBAT three position switch • Left position: board supplied by Jack connector • Middle position: board not supplied • Right position: board supplied by Phoenix connector
5	VBAT Phoenix connector
6	VPRE power supply
7	USB connectors (Open SDA for MCU flash; KL25Z for NXP GUI control)
8	Debug connectivity. Access to FS8600 signals
9	External regulator connectors (to VMONx)
10	VMONx configuration (choice between monitoring a regulator or a fixed 0.8 V)
11	OTP mode switch
12	DBG pin to 0 V if unplugged
13	Wake1 switch
14	VPRE compensation network settings (455 kHz or 2.22 MHz)
15	VDDI2C selection
16	KL25Z freedom board connectors

4.4.1 LED signaling

Figure 13 shows the LEDs provided as visual output devices for the evaluation board:

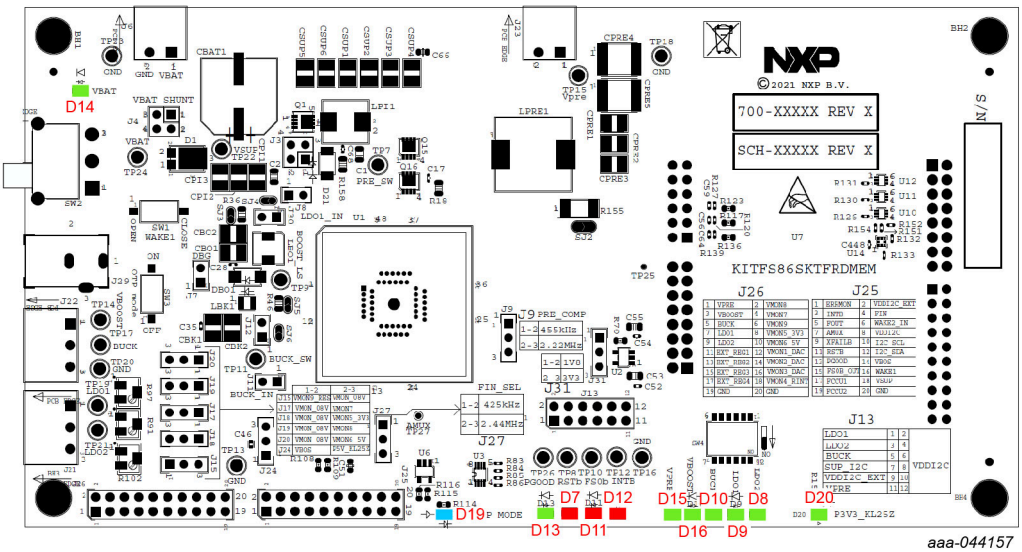

Figure 13. Evaluation board LED signaling location

Table 3. Evaluation board LED signaling description

Label	Name	Color	Description
D7	RSTB	Red	RSTB asserted (logic level = 0)
D8	LDO2	Green	LDO2 On
D9	LDO1	Green	LDO1 On
D10	BUCK	Green	BUCK On

Table 3. Evaluation board LED signaling description...*continued*

Label	Name	Color	Description
D11	FS0B	Red	FS0B asserted (logic level = 0)
D12	INTB	Red	INTB asserted (logic level = 0)
D13	PGOOD	Green	PGOOD released
D14	VBAT	Green	VBAT On
D15	VPRE	Green	VPRE On
D16	VBOOST	Green	VBOOST On
D19	DBG > 8.0 V	Blue	DBG pin voltage > 8.0 V (OTP programming)
D20	P3V3_KL25	Green	P3V3_KL25 On

4.4.2 Connectors

Figure 14 shows the location of connectors on the board.

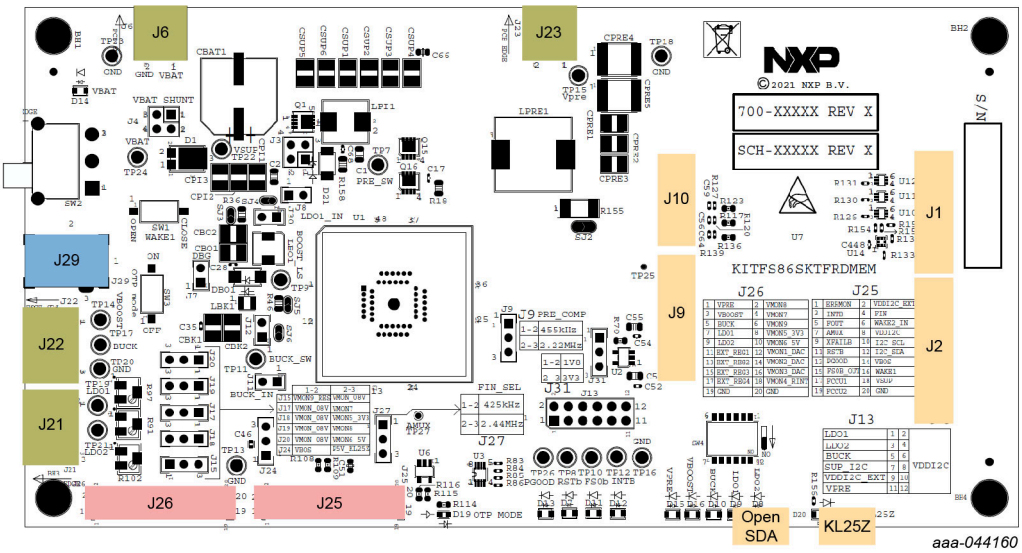

Figure 14. Evaluation board connectors location

4.4.2.1 VBAT connector (J6)

VBAT connects to the board through Phoenix connector (J6).

Table 4. VBAT Phoenix connector (J6)

Schematic label	Signal name	Description
J6-1	VBAT	Battery voltage supply input
J6-2	GND	Ground

4.4.2.2 Output power supply connectors

Table 5. LDO1/LDO2 connector (J21)

Schematic label	Signal name	Description
J21-1	LDO1	LDO1 power supply output
J21-2	LDO2	LDO2 power supply output

Table 5. LDO1/LDO2 connector (J21)*...continued*

Schematic label	Signal name	Description
J21-3	GND	Ground

Table 6. VBOOST/BUCK connector (J22)

Schematic label	Signal name	Description
J22-1	VBOOST	VBOOST output
J22-2	BUCK	BUCK power supply output
J22-3	GND	Ground

Table 7. VPRE connector (J23)

Schematic label	Signal name	Description
J23-1	VPRE	VPRE power supply output
J23-2	GND	Ground

4.4.2.3 Debug connector (J25)

Table 8. Debug connector (J25)

Schematic label	Signal name	Description
J25-1	ERRMON	Error monitoring
J25-2	VDDI2C_EXT	External VDDI2C voltage supply
J25-3	INTB	Interrupt PIN (active low)
J25-4	FIN	Frequency synchronization input
J25-5	FOUT	Frequency synchronization output
J25-6	WAKE2_IN	WAKE2 input
J25-7	AMUX	Analog multiplexer
J25-8	VDDI2C	VDDI2C pin voltage
J25-9	XFAILb	Power synchronization input/output with NXP low voltage PMIC
J25-10	I2C_SCL	I^2C serial clock
J25-11	RSTB	Reset pin (active low)
J25-12	I2C_SDA	I^2C serial data
J25-13	PGOOD	Power good
J25-14	VBOS	Best of supply
J25-15	FS0b_Out	Fail-safe pin (active low)
J25-16	WAKE1	Wake 1 pin voltage
J25-17	FCCU1	Fault collector control unit 1
J25-18	VSUP	VSUP power supply
J25-19	FCCU2	Fault collector control unit 2
J25-20	GND	Ground

4.4.2.4 Voltage monitoring connector (J26)

Table 9. Voltage monitoring connector (J26)

Schematic label	Signal name	Description
J26-1	VPRE	VPRE power supply output
J26-2	VMON8	Voltage monitoring input n°8
J26-3	VBOOST	VBOOST output
J26-4	VMON7	Voltage monitoring input n°7
J26-5	BUCK	BUCK power supply output
J26-6	VMON9	Voltage monitoring input n°9
J26-7	LDO1	LDO1 power supply output
J26-8	VMON5_3V3	Voltage monitoring input n°5
J26-9	LDO2	LDO2 power supply output
J26-10	VMON6_5V	Voltage monitoring input n°6
J26-11	n.c.	not connected
J26-12	VMON1_DAC	Voltage monitoring input n°1
J26-13	n.c.	not connected
J26-14	VMON2_DAC	Voltage monitoring input n°2
J26-15	n.c.	not connected
J26-16	VMON3_DAC	Voltage monitoring input n°3
J26-17	n.c.	not connected
J26-18	VMON4_RINT	Voltage monitoring input n°4
J26-19	GND	Ground
J26-20	GND	Ground

4.4.2.5 KL25Z Freedom board connectors

Table 10. Safety output connector (J1)

Schematic label	Signal name	Description
J1-1	n.c.	not connected
J1-2	INTB_MCU	Interruption (active low)
J1-3	n.c.	not connected
J1-4	RSTB_MCU	Reset (active low)
J1-5 → J1-9	n.c.	not connected
J1-10	FS0b_MCU	Fail-safe (active low)
J1-11 → J1-16	n.c.	not connected

Table 11. I^2C connector (J2)

Schematic label	Signal name	Description
J2-1 → J2-13	n.c.	not connected
J2-14	GND	Ground
J2-15 → J2-17	n.c.	not connected
J2-18	I2C_SDA_MCU	I^2C Serial Data line

Table 11. I^2C connector (J2)*...continued*

Schematic label	Signal name	Description
J2-19	n.c.	not connected
J2-20	I2C_SCL_MCU	I^2C Serial Clock line

Table 12. ADC connector (J10)

Schematic label	Signal name	Description
J10-1	VBOOST_ADC	BOOST power supply to KL25Z ADC
J10-2	DBG_ADC	DBG pin voltage to KL25Z ADC
J10-3	VPRE_ADC	VPRE power supply to KL25Z ADC
J10-4	AMUX_ADC	AMUX pin to KL25Z ADC
J10-5	BUCK_ADC	BUCK power supply to KL25Z ADC
J10-6	LDO1_ADC	LDO1 power supply to KL25Z ADC
J10-7	n.c.	not connected
J10-8	LDO2_ADC	LDO2 power supply to KL25Z ADC
J10-9	n.c.	not connected
J10-10	VBOS_ADC	VBOS pin voltage to KL25Z ADC
J10-11	n.c.	not connected
J10-12	VDDI2C_ADC	VDDI2C pin voltage to KL25Z ADC

Table 13. KL25Z supply connector (J14)

Schematic label	Signal name	Description
J14-1 → J14-3	n.c.	not connected
J14-4	P3V3_KL25Z	3.3 V generated from KL25Z
J14-5 → J14-7	n.c.	not connected
J14-8	P3V3_KL25Z	3.3 V generated from KL25Z
J14-9	n.c.	not connected
J14-10	P5V_KL25Z	5.0 V generated from USB
J14-11	n.c.	not connected
J14-12	GND	Ground
J14-13	n.c.	not connected
J14-14	GND	Ground
J14-15	n.c.	not connected
J14-16	n.c.	not connected

Table 14. KL25Z USB connectors

Schematic label	Signal name	Description
KL25Z	NA	USB connector used to communicate with the FS8600 part
Open SDA	NA	USB connector used to flash the KL25Z MCU

4.4.3 Test points

Figure 15 shows test points that provide access to various signals to and from the boards.

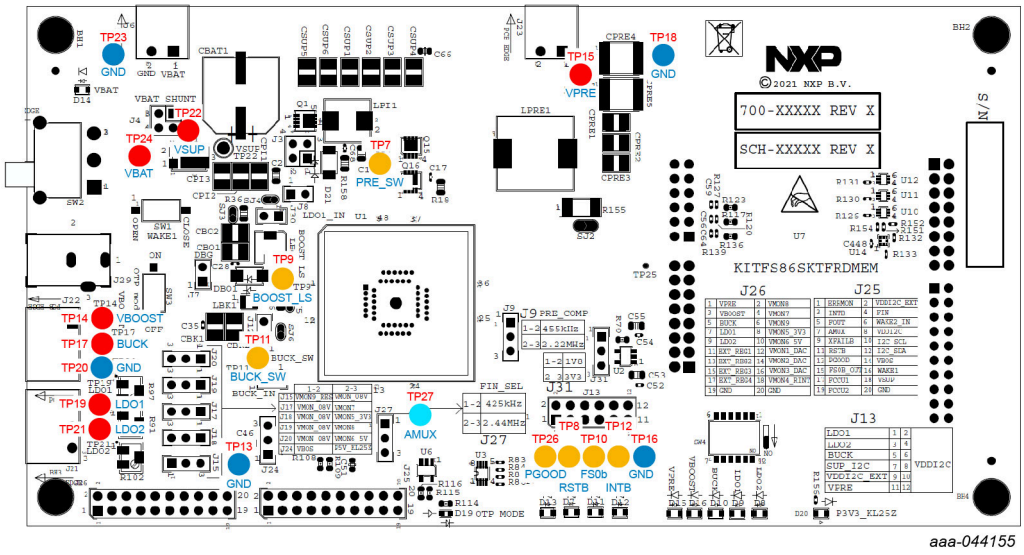

Figure 15. Evaluation board test points

Table 15. Evaluation board test points description

Test point name	Signal name	Description
TP7	PRE_SW	VPRE power supply switcher
TP8	RSTb	Reset pin (active low)
TP9	BOOST_LS	BOOST power supply low-side switcher
TP10	FS0b	Fail-safe pin (active low)
TP11	BUCK_SW	BUCK power supply switcher
TP12	INTB	Interruption pin (active low)
TP13	GND	Ground
TP14	VBOOST	BOOST power supply output
TP15	VPRE	VPRE power supply output
TP16	GND	Ground
TP17	BUCK	BUCK power supply output
TP18	GND	Ground
TP19	LDO1	LDO1 power supply output
TP20	GND	Ground
TP21	LDO2	LDO2 power supply output
TP22	VSUP	VSUP pin voltage
TP23	GND	Ground
TP24	VBAT	Battery voltage
TP27	AMUX	Analog MUX output

4.4.4 Jumpers

Figure 16 shows jumper locations for board configuration.

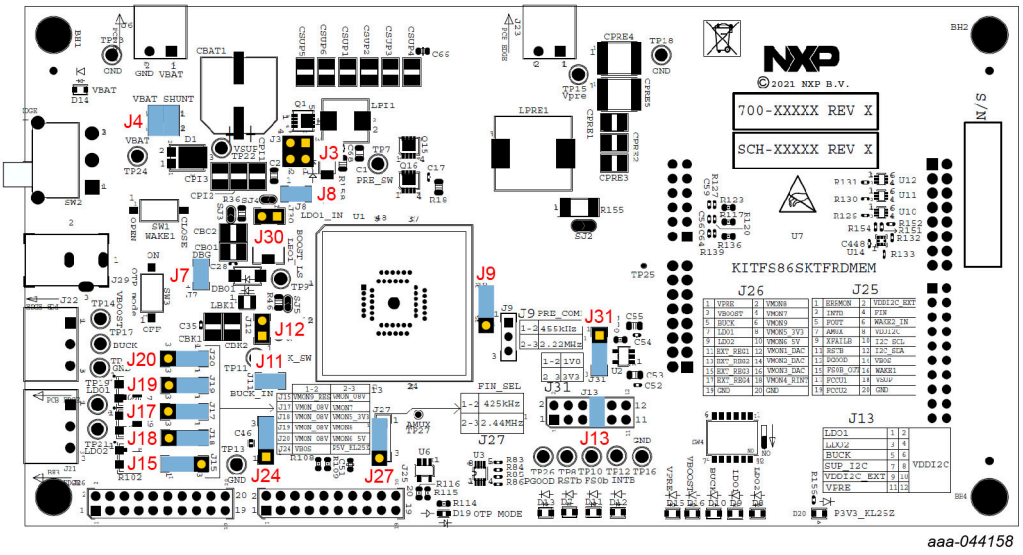

Figure 16. Evaluation board jumpers location (with default position)

Table 16. Evaluation board jumpers description

Name	Function	Pin number	Jumper/pin function
J3	BAT_SW shunt	1–2	Bypass BAT_SW protection
		3–4	Bypass BAT_SW protection
J4	VBAT shunt	1–2	Shunt switch SW1 for current > 5.0 A
		3–4	Shunt switch SW1 for current > 5.0 A
J7	Apply voltage to DBG pin	1–2	Either 5.0 V (DBG mode) or 8.0 V (OTP mode) depending on SW3 position
J8	LDO1 input	1–2	LDO1_IN tied to VPRE
J9	PRE_COMP selection	1–2	PRE_COMP for 455 kHz
		2–3	PRE_COMP for 2.2 MHz
J11	BUCK input	1–2	BUCK_IN tied to VPRE
J12	BUCK_SW shunt	1–2	For current measurement (insert current probe and remove SJ6)
J13	VDDI2C selection	1–2	VDDI2C tied to LDO1
		3–4	VDDI2C tied to LDO2
		5–6	VDDI2C tied to BUCK
		7–8	VDDI2C tied to SUP_I2C (onboard LDO)
		9–10	VDDI2C tied to VDDI2C_EXT (off-board supply)
		11–12	VDDI2C tied to VPRE
J15	VMON9_RES input selection	1–2	VMON9_RES/FIN pin tied to VMON9_RES (configured regulator through J25)
		2–3	VMON9_RES/FIN pin tied to VMON_08V (fixed 0.8 V)
J17	VMON7_RES input selection	1–2	VMON7_RES pin tied to VMON_08V (fixed 0.8 V)
		2–3	VMON7_RES pin tied to configured regulator (through J25)

Table 16. Evaluation board jumpers description...*continued*

Name	Function	Pin number	Jumper/pin function
J18	VMON5_RES input selection	1–2	VMON5_RES pin tied to VMON_08V (fixed 0.8 V)
		2–3	VMON5_RES pin tied to configured regulator (through J25)
J19	VMON8_RES input selection	1–2	VMON8_RES pin tied to VMON_08V (fixed 0.8 V)
		2–3	VMON8_RES pin tied to configured regulator (through J25)
J20	VMON6_RES input selection	1–2	VMON6_RES pin tied to VMON_08V (fixed 0.8 V)
		2–3	VMON6_RES pin tied to configured regulator (through J25)
J24	VMON_08V input selection	1–2	VMON_08V is generated by a LDO whose input is VBOS
		2–3	VMON_08V is generated by a LDO whose input is P5V_KL25Z
J27	External clock selection	1–2	Frequency = 425 kHz
		2–3	Frequency = 2.44 MHz
J30	VBOOST Inductor shunt	1–2	For current measurement (insert current probe and remove SJ4)
J31	SUP_I2C selection	1–2	SUP_I2C = 1.8 V
		2–3	SUP_I2C = 3.3 V

4.4.5 Switches

Figure 17 shows switches locations for board operation.

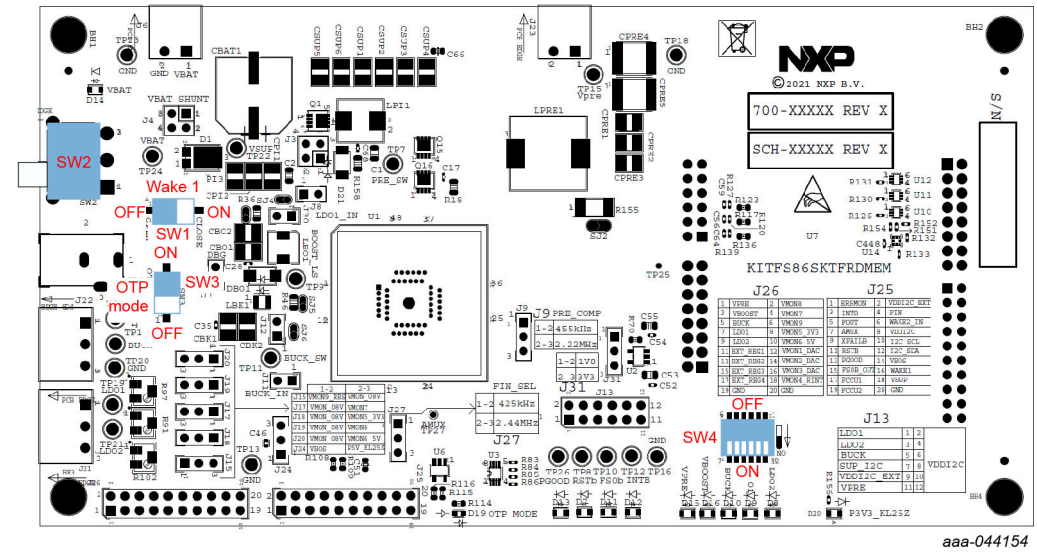

Figure 17. Switches location

Table 17. SW1 description

Position	Function	Description
RIGHT	Wake1 On	FS8600 can be powered up
LEFT	Wake1 Off	FS8600 cannot be powered up

Table 18. SW2 description

Position	Function	Description
TOP	VBAT On	VBAT from J6

Table 18. SW2 description...*continued*

Position	Function	Description
MIDDLE	VBAT Off	Board not supplied
BOTTOM	VBAT On	VBAT from J29

Table 19. SW3 description

Position	Function	Description
TOP	OTP mode On	FS8600 can be emulated or burnt by OTP
BOTTOM	OTP mode Off	FS8600 cannot be emulated or burnt by OTP

Table 20. SW4 description

Position	Function	Description
TOP	Corresponding LED Off	Each LED is controlled by an independent switch. Disconnecting them allows more accurate efficiency measurement.
BOTTOM	Corresponding LED On	

5 Configuring the hardware for startup

The device configuration can be changed twice. The programming steps are described in the NXP GUI for FS86 Automotive Family User Manual available at http://www.nxp.com/NXP GUI for Automotive PMIC Families.

Figure 18 presents a typical hardware configuration incorporating the development board, power supply and Windows PC workstation.

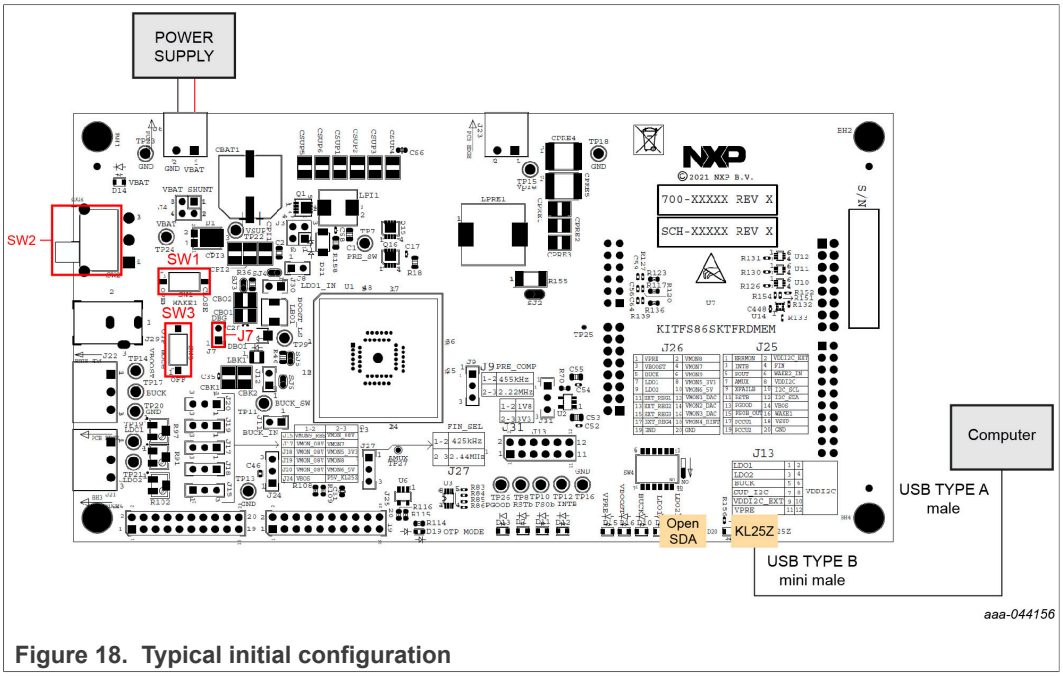

Figure 18. Typical initial configuration

To configure the hardware and workstation as illustrated in Figure 18, complete the following procedure:

1. Install jumpers and switches for the configuration shown in Table 21.

Table 21. Hardware configuration

Switch	Configuration		
	Normal mode	Debug mode entry	OTP mode entry
Operation	watchdog 2s window	watchdog window fully open	OTP emulation / programming and Debug mode entry
J7 (DBG)	open	connect 1 to 2 DBG pin voltage pulled to 4.5 V or 8.0 V (SW3)	
SW1 (WAKE1)	close (WAKE1 high)		
SW2 (VBAT)	middle position (VBAT OFF)		
SW3 (DBG_OTP)	open (DBG = 4.5 V)		close (OTP mode ON)

2. Connect the Windows PC USB port to the KITFS86SKTFRDMEM development board using the provided USB 2.0 cable.
3. Set the DC power supply to 12 V and current limit to 1.0 A. With power turned Off, attach the DC power supply positive and negative output to VBAT Phoenix connector (J6).
4. Turn On the power supply.
5. Put SW2 in TOP position.

At this step, if the product is in OTP mode entry configuration, all regulators are Off. The user can power up with an OTP configuration or configure the mirror registers before powering up. Power-up starts as soon as one of these four actions occurs:

- J7 jumper is removed
- SW3 is switched Off
- OTP mode exit command is sent by I^2C
- NXP GUI button "Exit OTP Mode" is clicked.

6 References

[1] **KITFS86SKTFRDMEM** — detailed information on this board, including documentation, downloads, and software and tools
http://www.nxp.com/KITFS86SKTFRDMEM

[2] **FS86** — detailed information on FS8600, Safety System Basis Chip For Domain Controller, Fit For ASIL B and D
http://www.nxp.com/FS86

[3] **NXP GUI for Automotive PMIC Families** — Software GUI for NXP's Automotive PMIC products
https://www.nxp.com/PMIC-GUI-SW

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