UM11668

KITFS86AUTFRDMEM evaluation board

Rev. 1 — 28 October 2021 **User manual**

Document information

Information	Content
Keywords	FS8600, KITFS86AUTFRDMEM, KL25Z, I2C
Abstract	The KITFS86AUTFRDMEM provides a development platform for evaluating the FS8600 family of devices. The kit can be connected to the NXP GUI software which allows users to read and modify device registers, try out OTP configurations, and burn the part.

Revision history

Revision history

Rev	Date	Description
v.1	20211028	• Initial version

Important notice

NXP provides the enclosed product(s) under the following conditions:

This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The goods provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end product incorporating the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. In order to minimize risks associated with the customers applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact NXP sales and technical support services.

1 Introduction

The KITFS86AUTFRDMEM evaluation board user manual is intended for the engineers involved in the evaluation, design, implementation, and validation of FS8600 fail-safe system basis chips with multiple SMPS and LDOs.

The KITFS86AUTFRDMEM provides a development platform for evaluating the FS8600 family of devices. The kit can be connected to the NXP GUI software which allows users to read and modify device registers, try out OTP configurations, and burn the part.

The KITFS86AUTFRDMEM is delivered with an empty OTP content in order to leave the opportunity to the user to burn the OTP configuration. The board contains a superset device (PFS8613AMDA0ES), allowing tests on all the FS8600 derivatives.

2 Finding kit resources and information on the NXP website

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on http://www.nxp.com.

The information page for KITFS86AUTFRDMEM evaluation board is at http://www.nxp.com/KITFS86AUTFRDMEM. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a Getting Started tab. The Getting Started tab provides quick-reference information applicable to using the KITFS86AUTFRDMEM evaluation board, including the downloadable assets referenced in this document.

Collaborate in the NXP community

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The NXP community is at https://community.nxp.com/.

3 Getting ready

Working with the KITFS86AUTFRDMEM requires the kit contents, additional hardware and a Windows PC workstation with installed software.

3.1 Kit contents

- Assembled and tested KITFS86AUTFRDMEM connected to a FRDM-KL25Z in an anti-static bag
- 3.0 ft USB-STD A to USB-B-mini cable
- Two connectors, terminal block plug, 2 pos., str. 3.81 mm
- Two connectors, terminal block plug, 3 pos., str. 3.81 mm
- Jumpers mounted on board
- Quick Start Guide

3.2 Additional hardware

In addition to the kit contents, the following hardware is necessary or beneficial when working with this kit.

- Power supply with a range of 8.0 V to 40 V and a current limit set initially to 1.0 A (maximum current consumption can be up to 6.0 A)

3.3 Windows PC workstation

This evaluation board requires a Windows PC workstation. Meeting these minimum specifications should produce great results when working with this evaluation board.

- USB-enabled computer with Windows 7 or Windows 10

3.4 Software

Installing software is necessary to work with this evaluation board. All listed software is available on the evaluation board's information page at http://www.nxp.com/KITFS86AUTFRDMEM or from the provided link.

- NXP GUI for automotive PMIC families - latest version

4 Getting to know the hardware

The KITFS86AUTFRDMEM provides flexibility to play with all the features of the device and make measurements on the main part of the application. The KL25Z MCU Freedom board mounted on the board, combined with the NXP GUI, allows access to the registers in read and write mode. All regulators are accessible through connectors. Nonuser signal, like DC/DC switcher node is mapped on test points. Digital signals (I^2C, RSTB, etc.) are accessible through connectors. Pin WAKE1 has a switch to control (Ignition) them. A VBAT switch is available to power On or Off the device and to choose the VBAT input connector.

The main purpose of this board is to evaluate FS8600 silicon in automotive applications.

This board can be operated in OTP mode or in DBG mode. OTP mode gives access to 2 sub-mode: Emulation mode and OTP fused mode.

- In Emulation mode, as long as the power is supplied and the device does not go into DEEP-FS, the board configuration stays valid.
- The OTP fused mode uses the fused configuration, the configuration will stay valid after a reboot of the device. The device can be fused twice.

4.1 Kit overview

The KITFS86AUTFRDMEM is a hardware evaluation tool that allows performance test. The FS8600 family can be evaluated with this board because it is populated with a superset part. The PFS8613xMDA0ES part soldered on the board can be fused twice.

An external LDO provides SUP_I2C voltage with a choice of 1.8 V or 3.3 V (default). SUP_I2C is intended to power FS86 I^2C communication. From USB voltage, an external DC-DC generates the OTP programming voltage (8.0 V) without any need for an external power supply.

An Emulation mode is available for testing as many configurations as needed. The voltage monitoring hardware configuration is done through resistors for VMON5 to VMON9. Note that this configuration can be changed by selecting the appropriate bridge resistors:

- VMON1_DAC: assigned to EXT_REG1 (no resistor bridge)

- VMON2_DAC: assigned to EXT_REG2 (no resistor bridge)
- VMON3_DAC: assigned to EXT_REG3 (no resistor bridge)
- VMON4_RINT: assigned to EXT_REG4 (no resistor bridge)
- VMON5_3V3: assigned to LDO1, 3.3 V (resistor bridge)
- VMON6_5V: assigned to LDO2, 5.0 V (resistor bridge)
- VMON7: assigned to BUCK (resistor bridge + potentiometer)
- VMON8: assigned to VPRE (resistor bridge + potentiometer)
- VMON9: assigned to BOOST (resistor bridge + potentiometer)

This configuration can be changed by installing appropriate resistor bridges. This board was designed to sustain up to 10 A total on V_{PRE}.

Layout is done using six layers PCB stack up and by following the rules for DC-DC converter layout design.

4.2 KITFS86AUTFRDMEM features

- VBAT power supply connectors (Jack and Phoenix)
- VPRE from 3.3 V to 5.0 V with output capability up to 10 A
- VBUCK from 1.0 V to 3.3 V
- VBOOST from 5.0 V to 6.0 V
- LDO1 from 1.5 V to 5.0 V
- LDO2 from 1.1 V to 5.0 V
- Ignition key switch
- FS0B external safety pin
- FRDM-KL25Z with embedded USB connection to NXP GUI for register access, OTP emulation, and programming (access to I^2C-bus, IOs, Debug, AMUX and regulators)
- LEDs that indicate signals and regulator status
- Support OTP fuse capabilities

4.3 Schematic, board layout and bill of materials

The schematic, board layout and bill of materials for the KITFS86AUTFRDMEM evaluation board are available at http://www.nxp.com/KITFS86AUTFRDMEM.

4.3.1 VMON board configuration

VMON1_DAC, VMON2_DAC, VMON3_DAC and VMON4_RINT use either DAC or internal resistor bridges (monitoring values are configurable by OTP for VMON4_RINT and VMONx_DAC). By default, VMON1-2-3_DAC are connected to a fixed 0.8 V supply (VMON_08V) through resistors R144, R145, and R146. VMON4_RES is disconnected from any power supply. This default configuration can be changed by disconnecting R144, R145, and R146 and using J12 to plug external power supplies. J12 is shown in Figure 1.

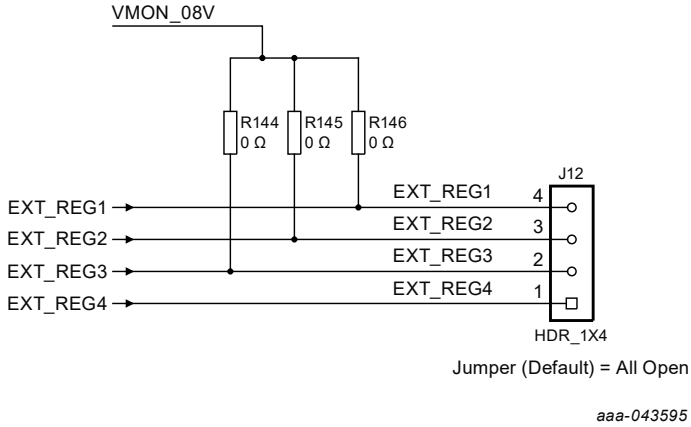

Figure 1. VMON1-2-3_DAC and VMON4_RINT inputs

VMON5_RES and VMON6_RES use external fixed resistor bridges to adapt the VMON input voltage to 0.8 V. Resistors bridges values were selected so that VMON5_RES and VMON6_RES would receive 0.8 V if VMONX_RES voltage inputs were respectively 3.3 V and 5.0 V. By default, VMON5_RES and VMON6_RES are respectively tied to LDO1 and LDO2. This can be changed by modifying R77 and R82 arrangement and soldering wires to the desired power supplies. Figure 2 and Figure 3 show the corresponding part of the schematic.

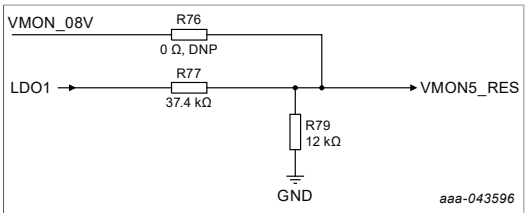

Figure 2. VMON5_RES input configuration

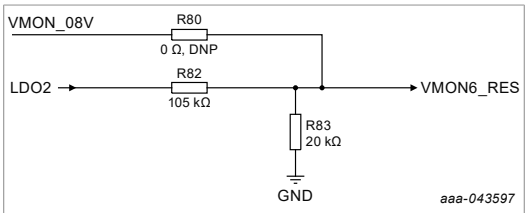

Figure 3. VMON6_RES input configuration

VMON7_RES, VMON8_RES and VMON9_RES are using potentiometers to adapt the VMON input voltage to 0.8 V by adjusting the resistor bridge depending on the connected regulator nominal voltage.

By default, VMON7_RES, VMON8_RES and VMON9_RES inputs are respectively connected to BUCK, BOOST and VPRE regulators. This configuration can be changed by modifying R128, R95, and R91 arrangement.

Figure 4 to Figure 6 show the corresponding parts of the schematic.

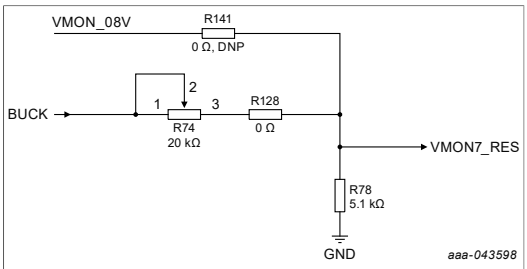

Figure 4. VMON7_RES input configuration

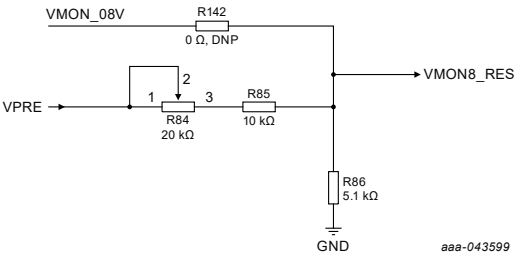

Figure 5. VMON8_RES input configuration

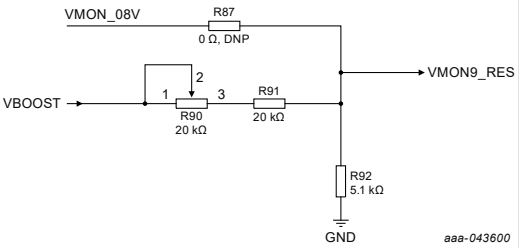

Figure 6. VMON9_RES input configuration

4.3.2 VPRE compensation network

This board is delivered with a VPRE compensation network defined for VPRE 4.1 V at 455 kHz. All other VPRE configurations (different voltage, output capacitors, inductor or current sense) require a new calculation for these components shown in Figure 7.

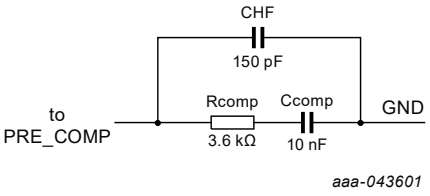

Figure 7. VPRE compensation network

Table 1 shows the recommendation for VPRE at both 455 kHz and VPRE 2.22 MHz.

Table 1. Compensation network

Components	VPRE 455 kHz	VPRE 2.22 MHz
CPRE	4x 22 µF	4x 10 µF
LPRE	4.7 µH	2.2 µH
Rsns	10 mΩ	10 mΩ
Rcomp	3.6 kΩ	4.7 kΩ
Ccomp	10 nF	3.3 nF
CHF	150 pF	33 pF

4.3.3 Battery switch

The FS8600 has a battery switch feature that disconnects the battery line from VPRE if the VPRE external high-side transistor is shorted. The battery switch functionality can be disabled by OTP. A PMOS is used to close the battery line at startup and open it in case of failure.

The transistor shown in Figure 6 must be bypassed if the function is not used.

The PMOS used has a maximum V_{DS} voltage of 40 V.

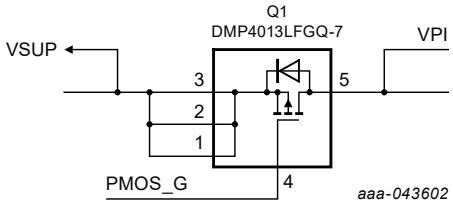

Figure 8. Battery switch

The PMOS gate is controlled by an external circuitry shown in Figure 7. An active solution using bipolar transistors is used to have better control performance. The objective is to have the fastest PMOS opening in case of VPRE HS failure.

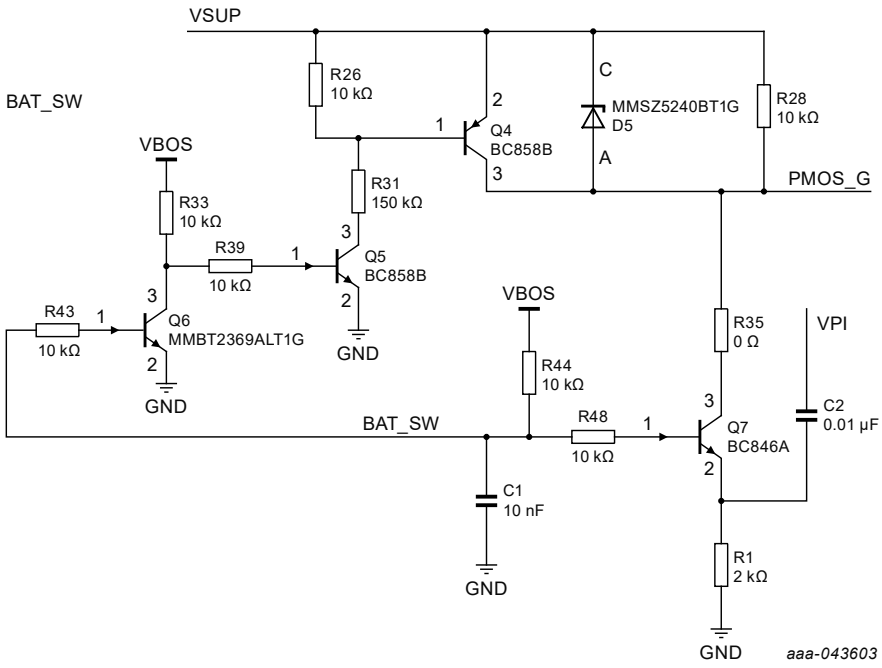

Figure 9. PMOS gate control circuitry

4.3.4 I²C

The I²C bus is connected to KL25Z MCU to communicate with NXP GUI. However, if the user wants to connect the I²C to another MCU, this is possible. In this case, remove R10 and R121 resistors to disconnect the KL25Z MCU (see Figure 10) and connect the external MCU on J25 connector as shown in Figure 11. In addition to this change, make sure that the VDDI2C voltage domain is the same on MCU side and SBC side.

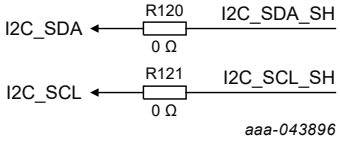

Figure 10. I²C connection to KL25Z

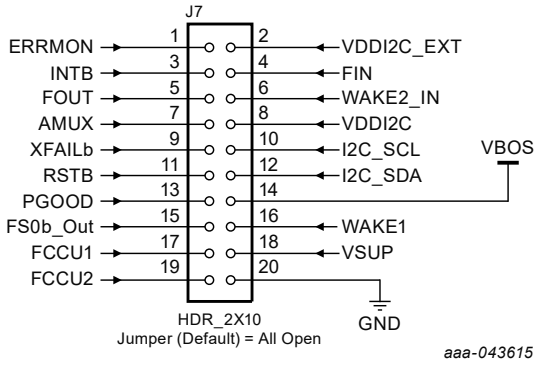

Figure 11. J7 I²C connection

4.3.5 VMON0_I2C

VMON0_I2C pin is powered through VDDI2C net and is used to supply internal buffers and I²C communication. The monitoring voltage needs to be selected by OTP due to an internal bridge.

The selection of VDDI2C is made using R34, R36, R40, R42, and R45 resistors shown in Figure 12. As an option, an external LDO is provided to feed VDDI2C through the VDDI2C_EXT net.

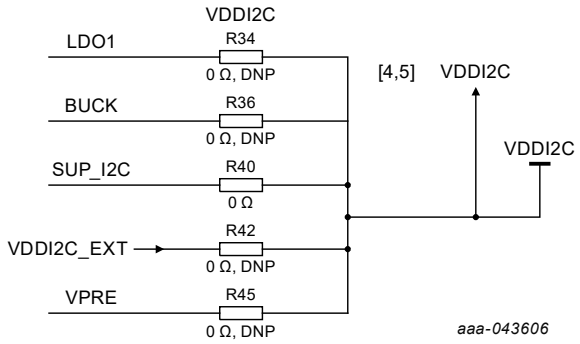

Figure 12. VDDI2C selection

The I²C is compatible with 1.8 V or 3.3 V, therefore SUP_I2C voltage is configurable between 3.3 V or 1.8 V using R37 and R38 (3.3 V by default) shown in Figure 13.

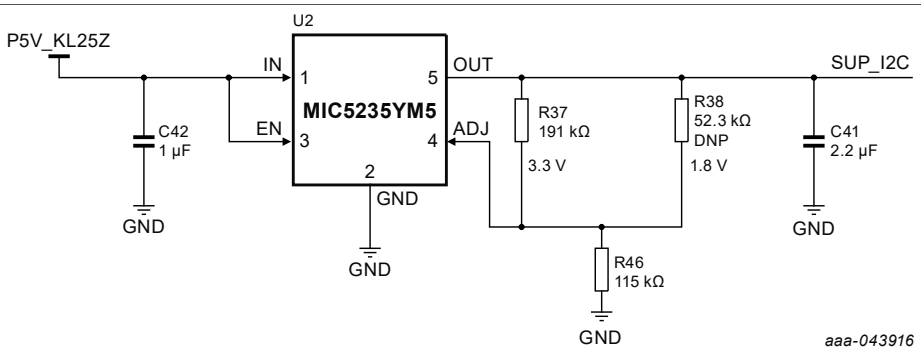

Figure 13. SUP_I2C supply

4.3.6 FIN external oscillator

In order to ease the FIN evaluation, a standalone oscillator is installed on the board. It supplies either 425 kHz or 2.4 MHz to the FIN input. The configuration is made using R68 and R137. Hardware implementation is shown in Figure 14.

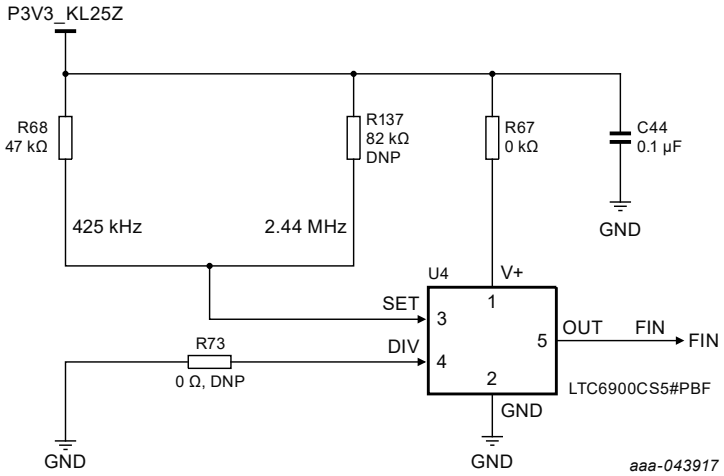

Figure 14. FIN oscillator

4.4 Kit featured components

Figure 15 identifies important components on the board and Table 2 provides additional details on these components.

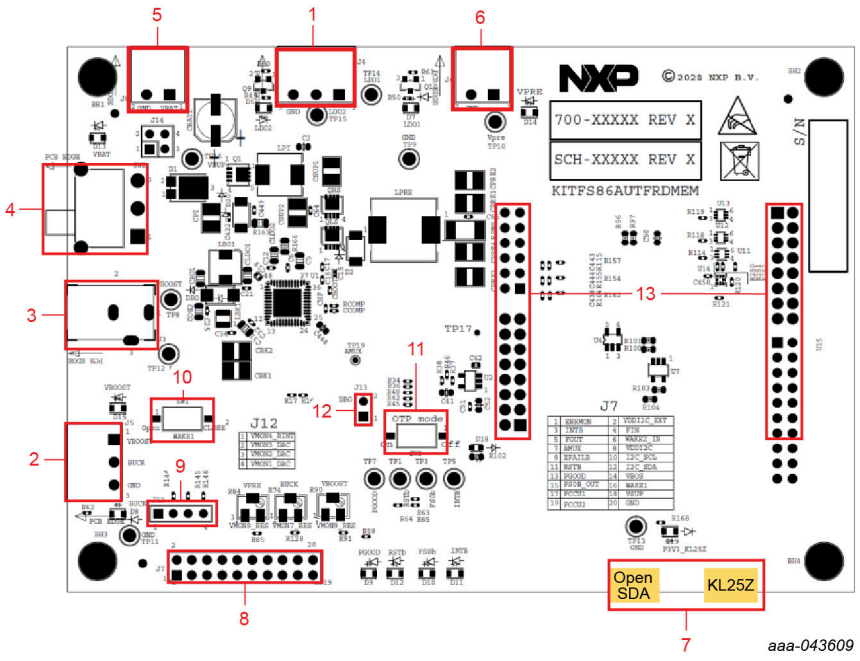

Figure 15. Evaluation board featured components location

Table 2. Evaluation board featured components location

Number	Description
1	LDO1/LDO2 power supply
2	BUCK/BOOST power supply
3	VBAT Jack connector
4	VBAT three position switch • Left position: board supplied by Jack connector • Middle position: board not supplied • Right position: board supplied by Phoenix connector
5	VBAT Phoenix connector
6	VPRE power supply
7	USB connectors (Open SDA for MCU flash ; KL25Z for NXP GUI control)
8	Debug connectivity. Access to FS8600 signals
9	External regulator connectors (to VMONx)
10	WAKE1 switch
11	OTP mode switch
12	DBG pin to 0 V if unplugged
13	KL25Z freedom board connectors

4.4.1 LED signaling

Figure 16 shows the LEDs provided as visual output devices for the evaluation board:

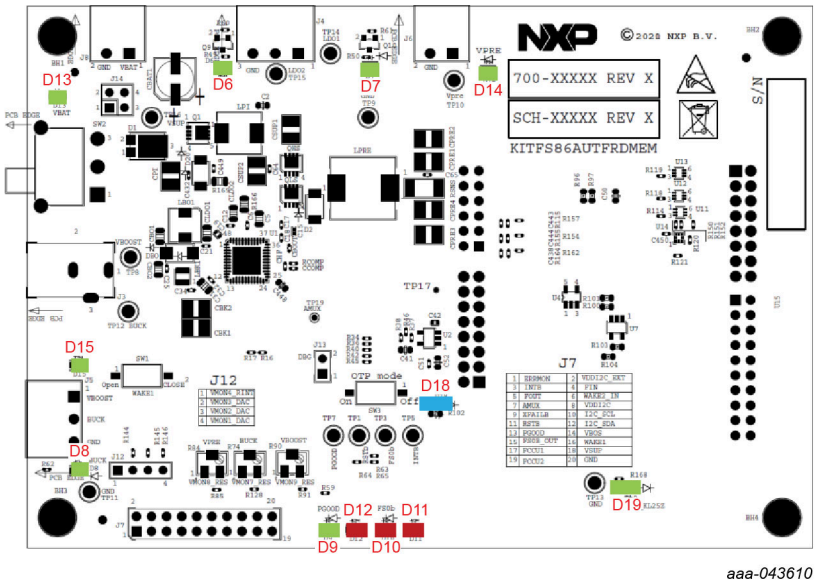

Figure 16. Evaluation board LED signaling location

Table 3. Evaluation board LED signaling location

Label	Name	Color	Description
D6	LDO2	Green	LDO2 On
D7	LDO1	Green	LDO1 On
D8	BUCK	Green	BUCK On

Table 3. Evaluation board LED signaling location...*continued*

Label	Name	Color	Description
D9	PGOOD	Green	PGOOD released
D10	FS0B	Red	FS0B asserted (logic level = 0)
D11	INTB	Red	INTB asserted (logic level = 0)
D12	RSTB	Red	RSTB asserted (logic level = 0)
D13	VBAT	Green	VBAT On
D14	VPRE	Green	VPRE On
D15	VBOOST	Green	VBOOST On
D18	DBG > 8.0V	Blue	DBG pin voltage > 8.0 V (OTP mode)
D19	P3V3_KL25	Green	P3V3_KL25 On

4.4.2 Connectors

Figure 17 shows the location of connectors on the board.

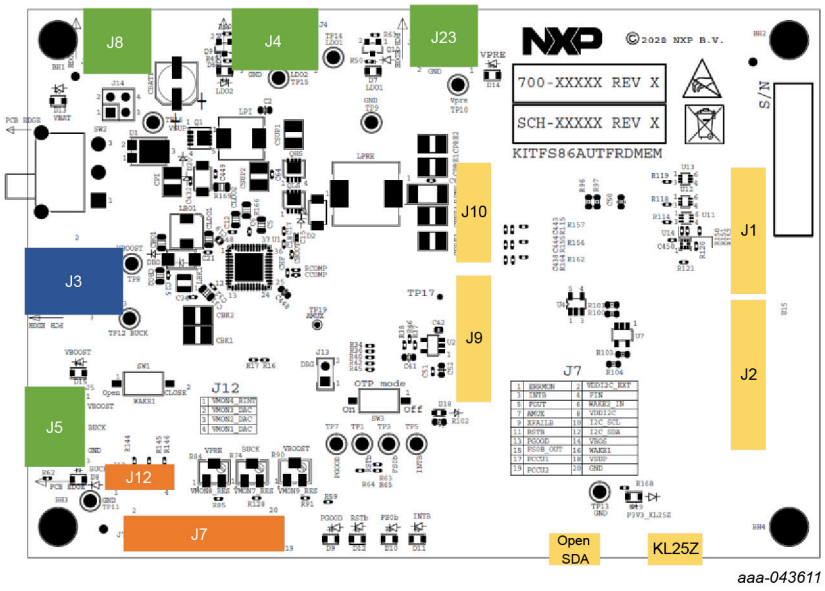

Figure 17. Evaluation board connectors location

4.4.2.1 VBAT connector (J8)

VBAT connects to the board through Phoenix connector (J8).

Table 4. VBAT Phoenix connector (J8)

Schematic label	Signal name	Description
J8-1	VBAT	Battery voltage supply input
J8-2	GND	Ground

4.4.2.2 Output power supply connectors

Table 5. LDO1/LDO2 connector (J4)

Schematic label	Signal name	Description
J4-1	LDO1	LDO1 power supply output

Table 5. LDO1/LDO2 connector (J4)*...continued*

Schematic label	Signal name	Description
J4-2	LDO2	LDO2 power supply output
J4-3	GND	Ground

Table 6. VBOOST/BUCK connector (J5)

Schematic label	Signal name	Description
J5-1	VBOOST	VBOOST output
J5-2	BUCK	BUCK power supply output
J5-3	GND	Ground

Table 7. VPRE connector (J23)

Schematic label	Signal name	Description
J23-1	VPRE	VPRE power supply output
J23-2	GND	Ground

4.4.2.3 Debug connector (J7)

Table 8. Debug connector (J7)

Schematic label	Signal name	Description
J7-1	ERRMON	Error monitoring
J7-2	VDDI2C_EXT	External supply for VMON0_I2C pin
J7-3	INTB	Interrupt, active low
J7-4	FIN	Frequency synchronization input
J7-5	FOUT	Frequency synchronization output
J7-6	WAKE2_IN	WAKE2 input
J7-7	AMUX	Analog multiplexer
J7-8	VDDI2C	VMON0_I2C pin voltage
J7-9	XFAILb	Power up sequencing pin voltage, active low
J7-10	I2C_SCL	I^2C serial clock
J7-11	RSTB	Reset pin voltage, active low
J7-12	I2C_SDA	I^2C serial data
J7-13	PGOOD	Power good
J7-14	VBOS	Best of supply pin voltage
J7-15	FS0b_Out	Fail-safe pin voltage, active low
J7-16	WAKE1	Wake 1 pin voltage
J7-17	FCCU1	Fault collector control unit 1
J7-18	VSUP	VSUP power supply
J7-19	FCCU2	Fault collector control unit 2
J7-20	GND	Ground

4.4.2.4 KL25Z Freedom board connectors

Table 9. Safety output connector (J1)

Schematic label	Signal name	Description
J1-1	n.c.	Not connected
J1-2	INTB_MCU	Interruption (active low)
J1-3	n.c.	Not connected
J1-4	RSTB_MCU	Reset (active low)
J1-5 → J1-9	n.c.	Not connected
J1-10	FS0b_MCU	Fail-safe (active low)
J1-11 → J1-16	n.c.	Not connected

Table 10. I^2C connector (J2)

Schematic label	Signal name	Description
J2-1 → J2-13	n.c.	Not connected
J2-14	GND	Ground
J2-15 → J2-17	n.c.	Not connected
J2-18	I2C_SDA_MCU	I^2C Serial Data line
J2-19	n.c.	Not connected
J2-20	I2C_SCL_MCU	I^2C Serial Clock line

Table 11. ADC connector (J10)

Schematic label	Signal name	Description
J10-1	VBOOST_ADC	BOOST power supply to KL25Z ADC
J10-2	DBG_ADC	DBG pin voltage to KL25Z ADC
J10-3	VPRE_ADC	VPRE power supply to KL25Z ADC
J10-4	AMUX_ADC	AMUX pin to KL25Z ADC
J10-5	BUCK_ADC	BUCK power supply to KL25Z ADC
J10-6	LDO1_ADC	LDO1 power supply to KL25Z ADC
J10-7	n.c.	Not connected
J10-8	LDO2_ADC	LDO2 power supply to KL25Z ADC
J10-9	n.c.	Not connected
J10-10	VBOS_ADC	VBOS pin voltage to KL25Z ADC
J10-11	n.c.	Not connected
J10-12	VDDI2C_ADC	VDDI2C pin voltage to KL25Z ADC

Table 12. KL25Z supply connector (J9)

Schematic label	Signal name	Description
J9-1 → J9-3	n.c.	Not connected
J9-4	P3V3_KL25Z	3.3 V generated from KL25Z
J9-5 → J9-7	n.c.	Not connected

Table 12. KL25Z supply connector (J9)*...continued*

Schematic label	Signal name	Description
J9-8	P3V3_KL25Z	3.3 V generated from KL25Z
J9-9	n.c.	Not connected
J9-10	P5V_KL25Z	5.0 V generated from USB
J9-11	n.c.	Not connected
J9-12	GND	Ground
J9-13	n.c.	Not connected
J9-14	GND	Ground
J9-15	n.c.	Not connected
J9-16	n.c.	Not connected

Table 13. KL25Z USB connectors

Schematic label	Signal name	Description
KL25Z	NA	USB connector used to communicate with the FS8600 part
Open SDA	NA	USB connector used to flash the KL25Z MCU

4.4.3 Test points

Figure 18 shows test points that provide access to various signals to and from the boards.

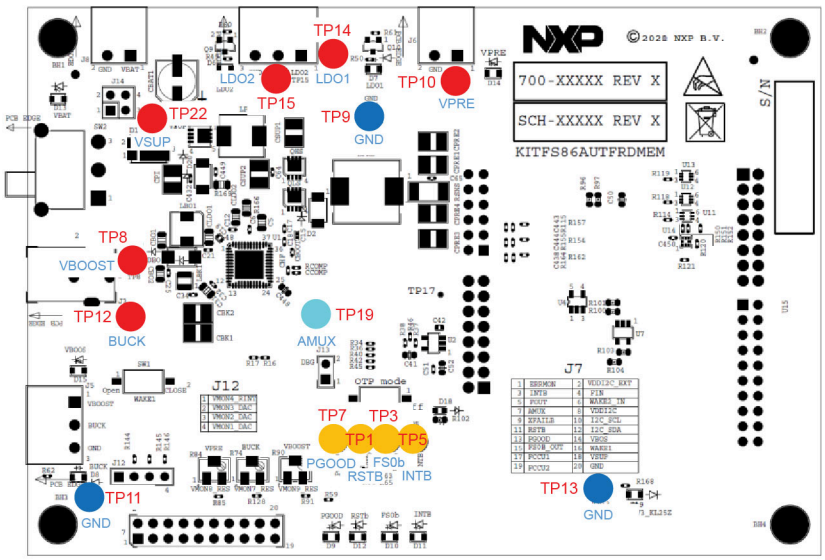

Figure 18. Evaluation board test points

Table 14. Evaluation board test points

Test point name	Signal name	Description
TP1	RSTB	Reset signal, active low
TP3	FS0B	Fail-safe output, active low
TP5	INTB	Interruption signal, active low

Table 14. Evaluation board test points...*continued*

Test point name	Signal name	Description
TP7	PGOOD	Power GOOD output, active low
TP8	VBOOST	VBOOS DC/DC output
TP9	GND	Ground
TP10	VPRE	VPRE power supply output
TP11	GND	Ground
TP12	BUCK	BUCK power supply output
TP13	GND	Ground
TP14	LDO1	LDO1 power supply output
TP15	LDO2	LDO2 power supply output
TP19	AMUX	Analog multiplexer
TP22	VSUP	VSUP pin voltage

4.4.4 Jumpers

Figure 19 shows jumper locations for board configuration.

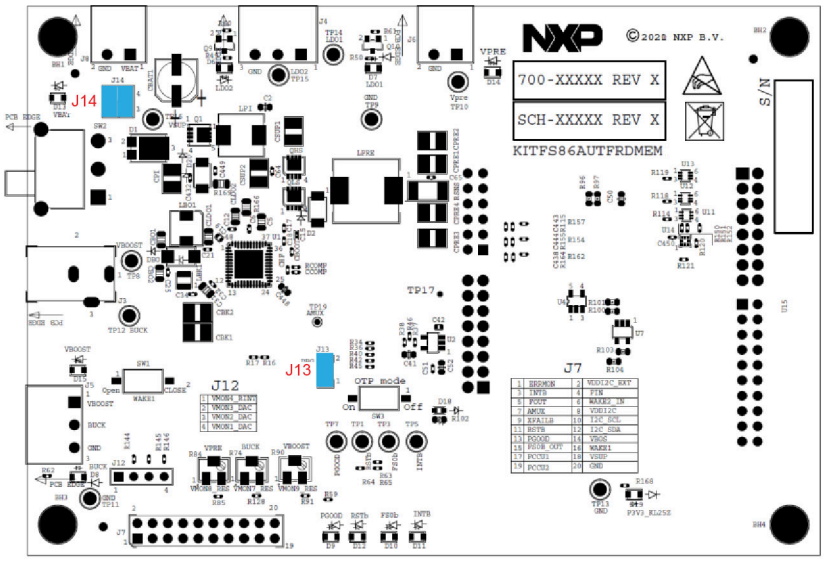

Figure 19. Evaluation board jumpers location (with default position)

Table 15. Evaluation board jumpers location (with default position)

Name	Function	Pin number	Jumper/pin function
J13	Apply voltage to DBG pin	1–2	DBG pin voltage pulled up to VBOS or 8.0 V depending on SW3 position
J14	VBAT shunt	1−2	Shunt switch SW1 for current > 5.0 A
		3−4	Shunt switch SW1 for current > 5.0 A

4.4.5 Switches

Figure 20 shows switches locations for board operation.

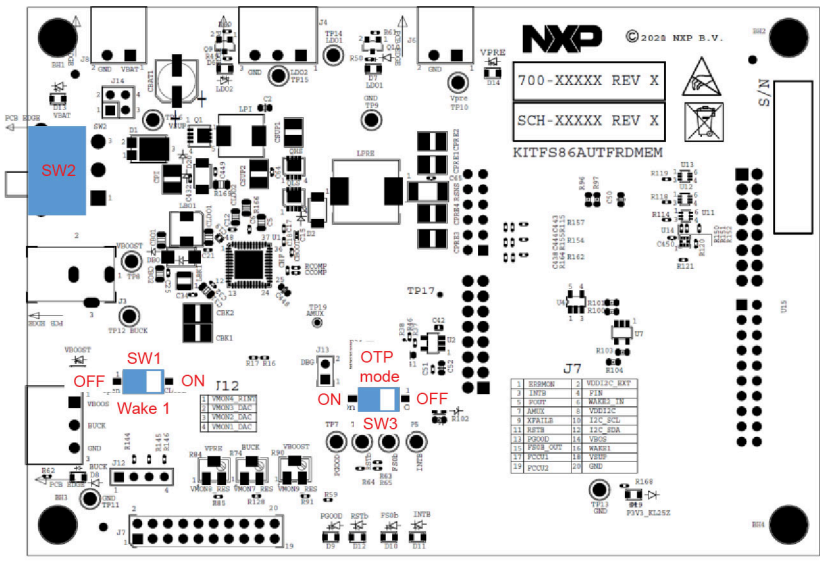

Figure 20. Switches location

Table 16. Switches location

Position	Function	Description
RIGHT	Wake1 On	FS8600 can be powered up
LEFT	Wake1 Off	FS8600 cannot be powered up

Table 17. SW2 description

Position	Function	Description
TOP	VBAT On	VBAT from J6
MIDDLE	VBAT Off	Board not supplied
BOTTOM	VBAT On	VBAT from J29

Table 18. SW3 description

Position	Function	Description
TOP	OTP mode On	FS8600 can be emulated or burnt by OTP
BOTTOM	OTP mode Off	FS8600 cannot be emulated or burnt by OTP

5 Configuring the hardware for startup

The device configuration can be programmed twice and emulated indefinitely using the GUI. Device programming and emulation steps are described in the NXP GUI for FS86 Automotive Family User Manual available at http://www.nxp.com/NXP GUI for Automotive PMIC Families.

Figure 21 presents a typical hardware configuration incorporating the development board, power supply and Windows PC workstation.

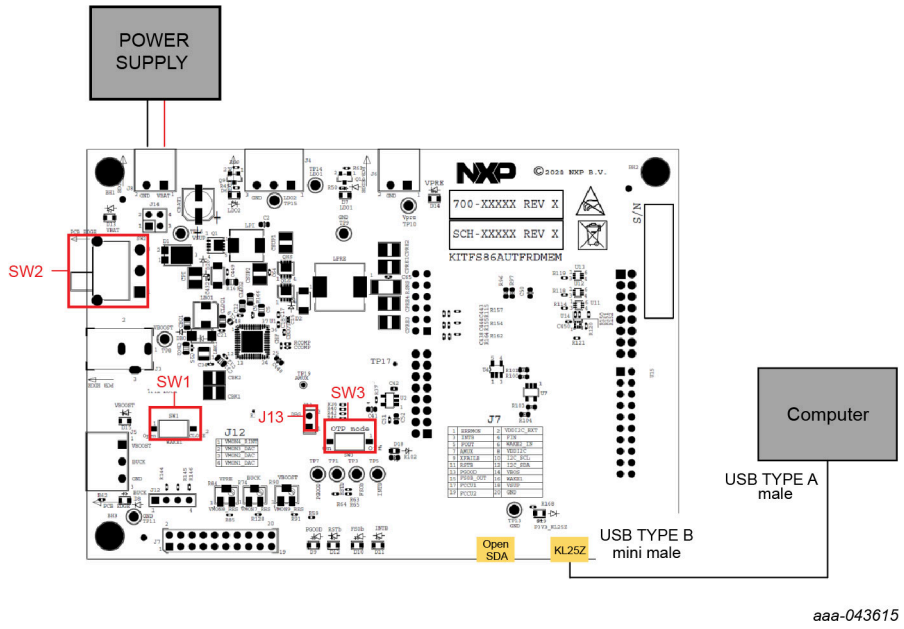

Figure 21. Typical initial configuration

To configure the hardware and workstation as illustrated in Figure 21, complete the following procedure:

1. Install jumpers and switches for the configuration shown in Table 19.

Table 19. Hardware configuration

Switch	Configuration		
	Normal mode	Debug mode entry	OTP mode entry
Operation	watchdog 2s window	watchdog window fully open	OTP emulation / programming and Debug mode entry
J13 (DBG)	open	connect 1 to 2 DBG pin voltage pulled to 4.5 V or 8.0 V (SW3)	
SW1 (WAKE1)	close (WAKE1 high)		
SW2 (VBAT)	middle position (VBAT OFF)		
SW3 (DBG_OTP)	open (DBG = 4.5 V)		close (OTP mode ON)

2. Connect the Windows PC USB port to the KITFS86AUTFRDMEM development board using the provided USB 2.0 cable.
3. Set the DC power supply to 12 V and current limit to 1.0 A. With power turned Off, attach the DC power supply positive and negative output to KITFS86AUTFRDMEM V_{BAT} Phoenix connector (J6).
4. Turn On the power supply.
5. Put SW2 in TOP position.

At this step, if the product is in OTP mode entry configuration, all regulators are Off. The user can power up with an OTP configuration or configure the mirror registers before powering up. Power-up starts as soon as one of these four actions occurs:

- J7 jumper is removed
- SW3 is switched Off
- OTP mode exit command is sent by I^2C
- NXP GUI button "Exit OTP Mode" is clicked

6 References

[1] **KITFS86AUTFRDMEM** — detailed information on this board, including documentation, downloads, and software and tools
http://www.nxp.com/KITFS86AUTFRDMEM

[2] **FS86** — detailed information on FS8600, Safety System Basis Chip For Domain Controller, Fit For ASIL B and D
http://www.nxp.com/FS86

[3] **NXP GUI for Automotive PMIC Families** — Software GUI for NXP's Automotive PMIC products
https://www.nxp.com/PMIC-GUI-SW

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