User's Guide
SLLU319–March 2020

Multipoint-Low Voltage Differential Signaling (M-LVDS) Evaluation Module

This document describes the multipoint low-voltage differential-signaling (M-LVDS) evaluation module (EVM) used to aid designers in development and analysis of this signaling technology. The Texas Instruments SN65MLVD200B, SN65MLVD201, SN65MLVD202B, SN65MLVD203B, SN65MLVD204B, SN65MLVD205B, SN65MLVD206, and SN65MLVD207 series are low-voltage differential line drivers and receivers complying with the M-LVDS standard (TIA/EIA−899). The EVM kit contains the assembled printed-circuit board and the SN65MLVD203B and SN65MVD204BRUM installed. The rest of the released devices referred to in Table 1 are supported by the EVM but need to be ordered and installed seperately. Using the EVM to evaluate these devices should provide insight into the design of low-voltage differential circuits. The EVM board allows the designer to connect an input to one or both of the drivers and configure a point-to-point, multidrop, or multipoint data bus.

The EVM can be used to evaluate device parameters while acting as a guide for high-frequency board layout. The board allows for the connection of a 100-Ω controlled impedance cable of varying lengths. This provides the designer with a tool for evaluation and successful design of an end product.

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1 The M-LVDS Evaluation Module

1.1 Overview

The EVM comes with all the production devices in Table 1. The SN65MLVD203B and SN65MLVD204B in the RUM package are installed on the circuit board. The other M-LVDS devices evaluated with this EVM are in the SN75ALS180 and SN75176 footprint. Use of these industry standard footprints allows the designer to easily configure the parts into a simplex or half-duplex data bus. These are all TIA/EIA−899 M-LVDS standard compliant devices. While initially intended for half-duplex or multipoint applications, M-LVDS devices are not precluded from being used in a point-to-point or multidrop configuration. In these configurations a distinct advantage is gained by the additional current drive provided by an M-LVDS driver.

The M-LVDS devices shown in Table 1 all include output slew-rate limited drivers, thus the need for different nominal signaling rates. The M-LVDS standard recommends the transition time not exceed 0.5 of the unit interval (UI). The definition of transition time (t_r and t_f) in M-LVDS is the 10% to 90% levels shown in Figure 1. Using the maximum transition time for each of the drivers and the 0.5(t_{UI}) *rule* results in the signaling rates shown in Table 1. This slew-rate control differentiates M-LVDS devices from LVDS (TIA/EIA−644A) compliant devices. The slower transition times available with M-LVDS help to reduce higher frequency components in the transmitted signal. This reduces EMI and allows longer stubs on the main transmission line. For this reason it is generally better to select a driver with a specified signaling rate no greater than is required in the system.

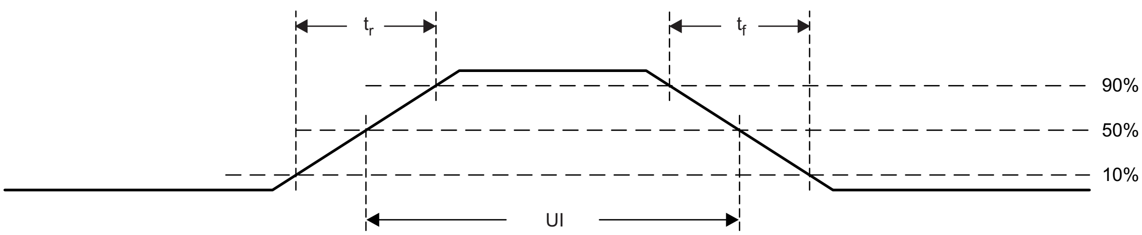


Figure 1. M-LVDS Unit Interval Definition

Table 1. M-LVDS Devices Supported by the EVM

Nominal Signaling Rate (Mbps	Footprints	Receiver Type	Part Number
100	SN75176	Type-1	SN65MLVD200AD
200	SN75176	Type-1	SN65MLVD201D
100	SN75ALS180	Type-1	SN65MLVD202AD
200	SN75ALS180	Type-1	SN65MLVD203D
100	SN75176	Type-2	SN65MLVD204AD
100	SN75ALS180	Type-2	SN65MLVD205AD
200	SN75176	Type-2	SN65MLVD206D
200	SN75ALS180	Type-2	SN65MLVD207D

The EVM has been designed with the individual driver and receiver section (U1) on one half of the board and the transceiver section (U3) on the other half in the RUM package. U2 and U4 are uninstalled by default, but can be installed if evaluating the devices in Table 1 is desired (see Figure 12). The EVM as delivered incorporates one 100-Ω termination resistor at each driver output, receiver input, and transceiver I/O. This allow the user to evaluate a single driver, receiver, or transceiver, connected together on the same EVM while not having to deal with a transmission line or additional I/Os. The EVM has an additional, uninstalled 100-Ω termination resistor at each driver output, receiver input, and transceiver I/O that can be installed depending on the desired configuration. Additionally, each receiver output will be one-tenth of the actual value if measured at the SMA connector due to the 453-Ω resistor in series with the output. The resistor is installed as a current limit for termination into a 50-Ω load.

Jumpers are included to allow the two sections of the EVM to either share the same power and ground or be run off of independent supplies. Ground shifts or common-mode offsets can be introduced by the removal of these jumpers and using separate power supplies.

1.2 M-LVDS Standard TIA/EIA−899

The M-LVDS standard was created in response to a demand from the data communications community for a general-purpose high-speed balanced interface standard for multipoint applications. The TIA/EIA−644 standard defines the LVDS electrical-layer characteristics used for transmitting information in point-to-point and multidrop architectures. TIA/EIA−644 does not address data transmission for multipoint architectures, therefore the need for development of a new standard.

The standard, Electrical Characteristics of Multipoint-Low-Voltage Differential Signaling (M-LVDS) TIA/EIA−899, specifies low-voltage differential signaling drivers and receivers for data interchange across half-duplex or multipoint data bus structures. M-LVDS is capable of operating at signaling rates up to 500 Mbps. In other words, when the devices are used at the nominal signaling rate, the rise and fall times will be within the specified values in the standard. The M-LVDS standard defines the transition time (t_r and t_f) to be 1 ns or slower into a test load. Using this information combined with the requirement that the transition time not exceed 0.5 of the unit interval (UI), gives a minimum unit interval of 2 ns, leading to the 500 Mpbs maximum signaling rate.

The standard defines Type-1 and Type-2 receivers. Type-1 receivers include no provisions for failsafe and have their differential input voltage thresholds near zero volts. Type-2 receivers have their differential input voltage thresholds offset from zero volts to detect the absence of a voltage difference. Type-1 receivers maximize the differential noise margin and are intended for the maximum signaling rate. Type-2 receivers are intended for control signals, slower signaling rates, or where failsafe provisions are needed. The bus voltage logic state definition can be seen in Table 2 and Figure 2.

Table 2. Receiver Input Voltage Threshold Requirements

Receiver Type	Low	High
Type-1	$-2.4\text{ V} \leq V_{ID} \leq -0.05\text{ V}$	$0.05\text{ V} \leq V_{ID} \leq 2.4\text{ V}$
Type-2	$-2.4\text{ V} \leq V_{ID} \leq 0.05\text{ V}$	$0.15\text{ V} \leq V_{ID} \leq 2.4\text{ V}$

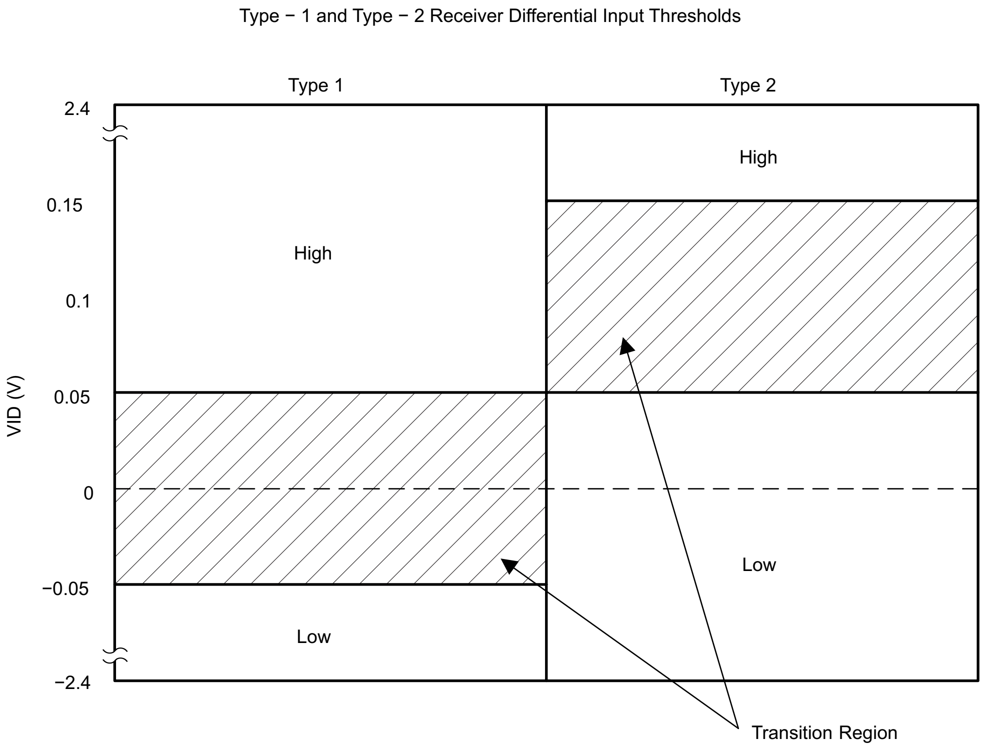


Figure 2. Expanded Graph of Receiver Differential Input Voltage Showing Transition Region

1.3 M-LVDS EVM Kit Contents

The M-LVDS EVM kit contains the following:

- M-LVDS EVM PCB with SN65MLVD203BRUM and SN65MLVD204BRUM installed

1.4 Configurations

The M-LVDS EVM board allows the user to construct various bus configurations. The two devices on the EVM allow for point-to-point simplex, parallel-terminated point-to-point simplex, and two-node multipoint operation. All of these modes of operation can be configured through onboard jumpers, external cabling, and different resistor combinations. The devices which are delivered with the EVM change output operation but, configuration of jumpers to setup the transmission type is independent of the devices installed

1.4.1 Point-to-Point

The point-to-point simplex configuration is shown in Figure 3. The setup schematic for this option is shown in Figure 9. Although this is not the intended mode of operation for M-LVDS, it works well for high noise or long higher-loss transmission lines. Due to the increased drive current, a single 100-Ω termination resistor on the EVM will result in a differential bus voltage (V_{OD}) twice as large as a doubly terminated line. This practice is acceptable as long as the combination of input voltage and common-mode voltage does not exceed absolute maximum ratings of the line circuits.

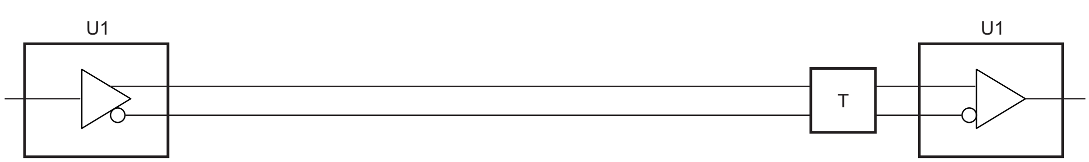


Figure 3. Point-to-Point Simplex Circuit

This configuration can also have a termination at the source and load (parallel terminated), thereby, keeping normal M-LVDS signal levels as shown in Figure 4.

The schematic for this option is shown in Figure 10. Due to the increased drive current, double termination can be used to improve transmission line characteristics .

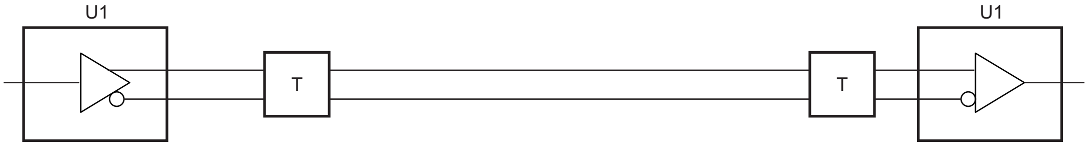


Figure 4. Parallel Termination Simplex Circuit

1.4.2 Multidrop

A multidrop configuration (see Figure 5) with two receiver nodes can be simulated with the EVM. To get additional receiver nodes on the same bus requires additional EVMs. M-LVDS controlled driver transition times and higher signal levels help to accommodate the multiple stubs and additional loads on the bus. This does not exempt good design practices, which would keep stubs short to help prevent excessive signal reflections.

A bus line termination could be placed at both ends of the transmission line, improving the signal quality by reducing return reflections to the driver. This would allow the use of standard compliant TIA/EIA 644A receivers on the bus in addition to M-LVDS receivers.

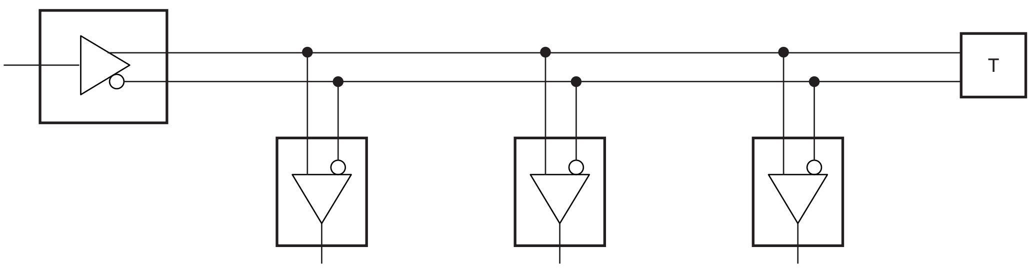


Figure 5. Multidrop or Distributed Simplex Circuit

1.4.3 Multipoint

The multipoint configuration is the primary application of the M-LVDS devices and the associated standard. The M-LVDS standard allows for any combination of drivers, receivers, or transceivers up to a total of 32 on the line.Figure 6 shows a representation of a five-node multipoint configuration using transceivers. Increased drive current, in addition to the wider common- mode input, allows M-LVDS parts to drive multiple receivers over longer line lengths with up to 2 V of ground noise.

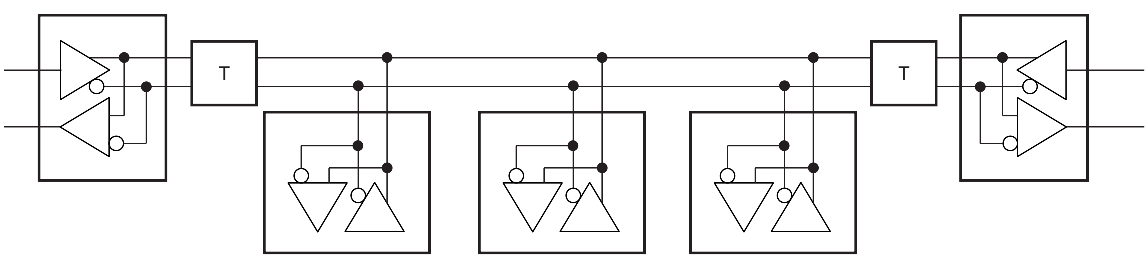


Figure 6. Five-Node Multipoint Circuit

A two-node multipoint setup (see Figure 7) can be configured with the EVM. Additional EVMs are needed for more nodes. The test setup and schematic for this configuration is shown in Figure 11.

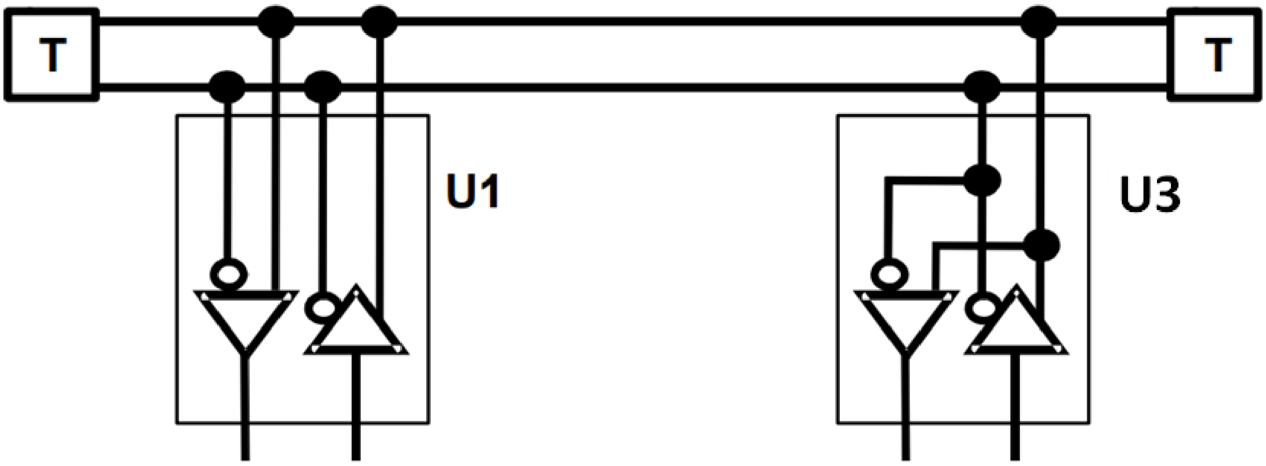


Figure 7. Two-Node Multipoint Circuit

1.4.4 EVM Operation With Separate Power Supplies

The EVM has been designed with independent power planes for the two devices. The two devices can be powered with independent supplies or with a single supply. Sending and receiving data between backplanes, racks, or cabinets where separate power sources may exist can have offset ground potentials between nodes. Jumpers JMP9, 10, 11, and 12 tie the two separate power and ground planes together. If two separate supplies are used and jumpers JMP9, 10, 11, and 12 are removed, care should be taken to ensure the absolute maximum device ratings are not exceeded. Keep in mind that if jumpers JMP9, 10, 11, and 12 are not removed when using separate power supplies, a difference in potential between the supplies causes a current to flow between supplies and through the jumpers.

The EVM can be configured with three power supplies with isolated outputs in such a way as to input a fixed offset between the grounds (see Figure 8). This induces a ground potential difference voltage between U1 and U3. To demonstrate this capability, the following steps should be followed.

1. Adjust PS1 and PS3 to the supply voltage (3.3 V) and current limit to 50 mA.
2. Set PS2 to 0 V
3. Induce a ground offset by varying the output of PS2.

WARNING

PS2 Output

The PS2 output should not exceed ±2 V to remain within the device ratings.

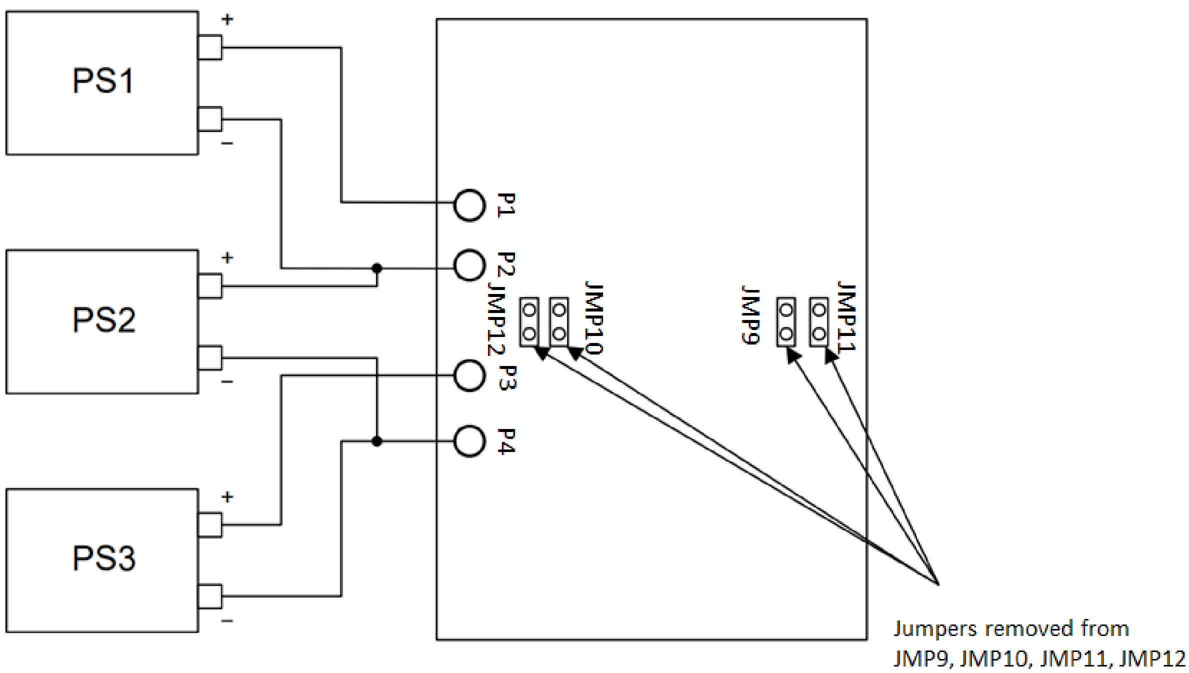


Figure 8. EVM Configuration for Including a Ground Potential Difference Voltage Between Nodes

1.5 Recommended Equipment

- 3.3 Vdc at 0.5-A power supply or multiple power supplies (with both devices powered and enabled the board draws about 35 mA).
- A 100-Ω transmission medium from the driver to the receiver, (twisted-pair cable recommended, CAT5 cable for example).
- SMA cables
- A function or pattern generator capable of supplying 3.3-V signals at the desired signaling rate.
- A multiple-channel high-bandwidth oscilloscope, preferably above the 1-GHz range
- Differential or single ended oscilloscope probes.

2 Test Setup

This chapter describes how to setup and use the M-LVDS EVM.

2.1 Typical Cable Test Configurations

Each of the following test configurations is a transmission line consisting of a twisted-pair cable connected on the 2-pin connectors (P1, P2, or P3). Table 3 shows the possible configurations.

In addition to the different transmission topologies, the EVM can also be configured to run off two or three separate power supplies, as described in the previous section. This would allow the user to induce a ground shift or offset between the two different drivers and receivers. This setup can be used with any transmission line test.

Table 3. EVM Configuration Options

Configuration	Jumpers In	Resistors In	Resistors Out	Diagram
Point-to-point simplex transmission	JMP1, 2, 9, 10, 11 ,12	R5	R4, 6, 8, 10, 11, 12, 13	Figure 9

Table 3. EVM Configuration Options (continued)

Configuration	Jumpers In	Resistors In	Resistors Out	Diagram
Point-to-point parallel terminated simplex transmission	JMP1, 2, 9, 10, 11, 12	R5, 11	R4, 6, 8, 10, 12, 13	Figure 10
Two-node multipoint transmission	JMP1, 2, 5, 6, 9, 10, 11, 12	R6, 32	R4, 5, 8, 10, 11, 13, 30 31, 35	Figure 11

2.1.1 Point-to-Point Simplex Transmission

1. Connect a twisted-pair cable from W1 to W2.
2. Verify resistor R5 is installed.
3. Remove resistors R6, R11, and R12. This properly terminates the transmission line at one end. Also remove resistors R4, R8, R10, and R13 leading to the SMA connectors.
4. Enable the driver by connecting the jumper on JMP2 between pin 1 and pin 2, or U1 pin 3 to V_{CC}.
5. Enable the receiver by connecting the jumper on JMP1 between pin 2 and pin 3, or U1 pin 2 to GND.

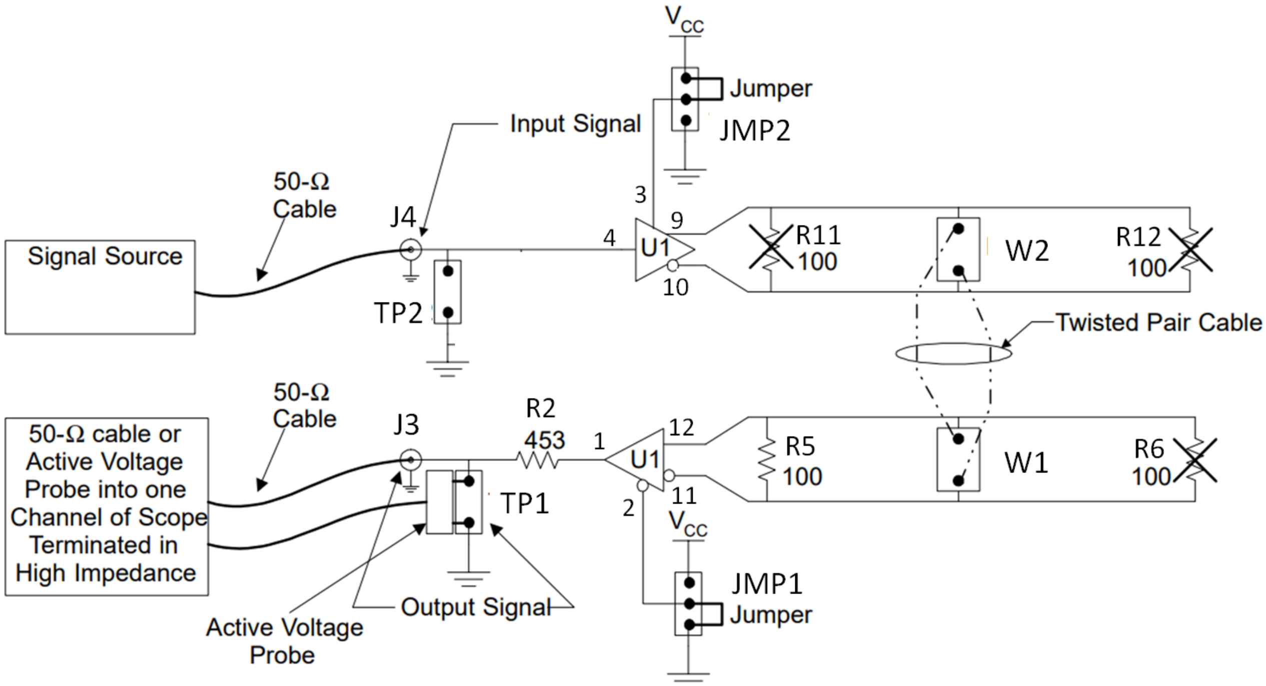


Figure 9. Point-to-Point Simplex Transmission

2.1.2 Point-to-Point Parallel Terminated Simplex Transmission

1. Connect a twisted-pair cable from W1 to W2.
2. Verify resistorS R5 and R11 are installed.
3. Remove resistors R6 and R12. This properly terminates the transmission line at both ends. Also remove resistors R4, R8, R10, and R13 leading to the SMA connectors.
4. Enable the driver by connecting the jumper on JMP2 between pin 1 and pin 2, or U1 pin 3 to V_{CC}.
5. Enable the receiver by connecting the jumper on JMP1 between pin 2 and pin 3, or U1 pin 2 to GND.

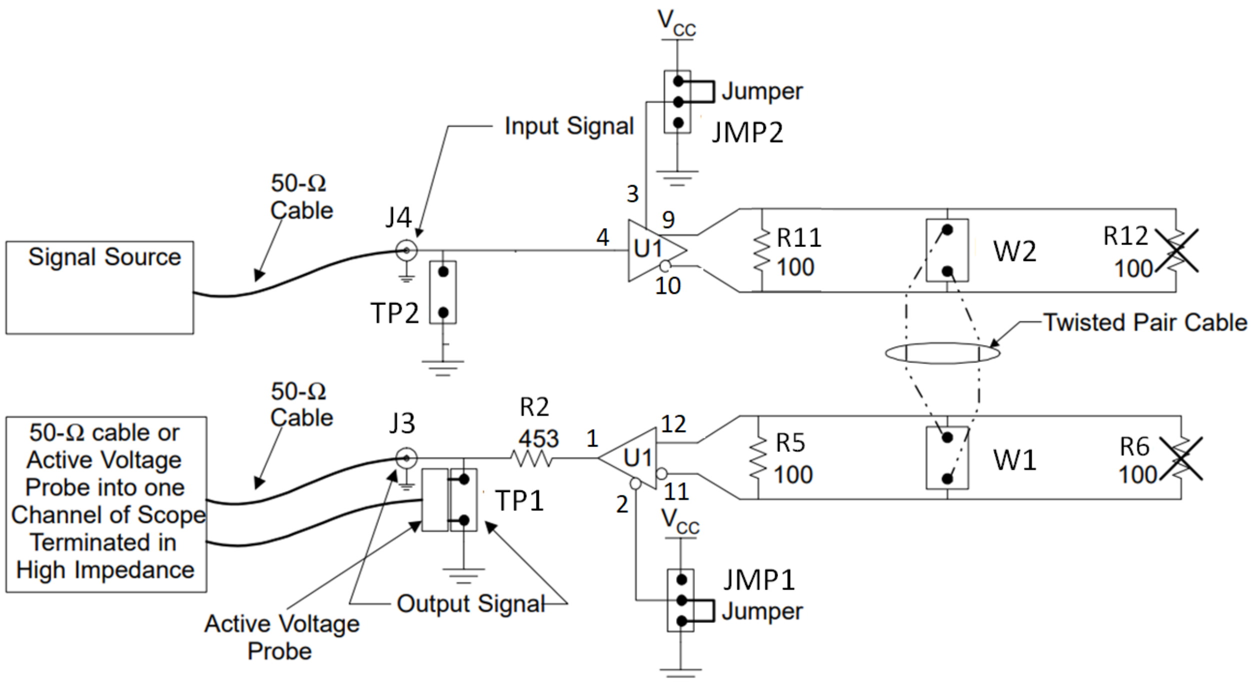


Figure 10. Point-to-Point Parallel Terminated Simplex Transmission

2.1.3 Two-Node Multipoint Transmission

1. Connect a twisted-pair cable between W1, W2, and W5.
2. Verify resistor R6 and R32 are installed.
3. Remove resistors R5, R11, R12, and R31. This properly terminates the transmission line at both ends.Also remove resistors R4, R8, R10, R13, R30, and R35 leading to the SMA connectors.
4. Enabling the driver in a two-node multipoint configuration will be a slightly more challenging task. The user can either jumper enable a single driver and send all of the data on the bus through a single driver, or sync the driver enable to the data and send data from each driver. Enable a single driver by connecting the jumper on JMP6 between pin 1 and pin 2 which connects U3 pin 3 to V_{CC}, or by connecting the jumper on JMP2 between pin 1 and pin 2 which connects U1 pin 3 to V_{CC}.
5. Enable the receivers by connecting the jumpers on JMP1 and JMP5 between pin 2 and pin 3, or U1 pin 2 to GND and U2 pin 2 to GND.

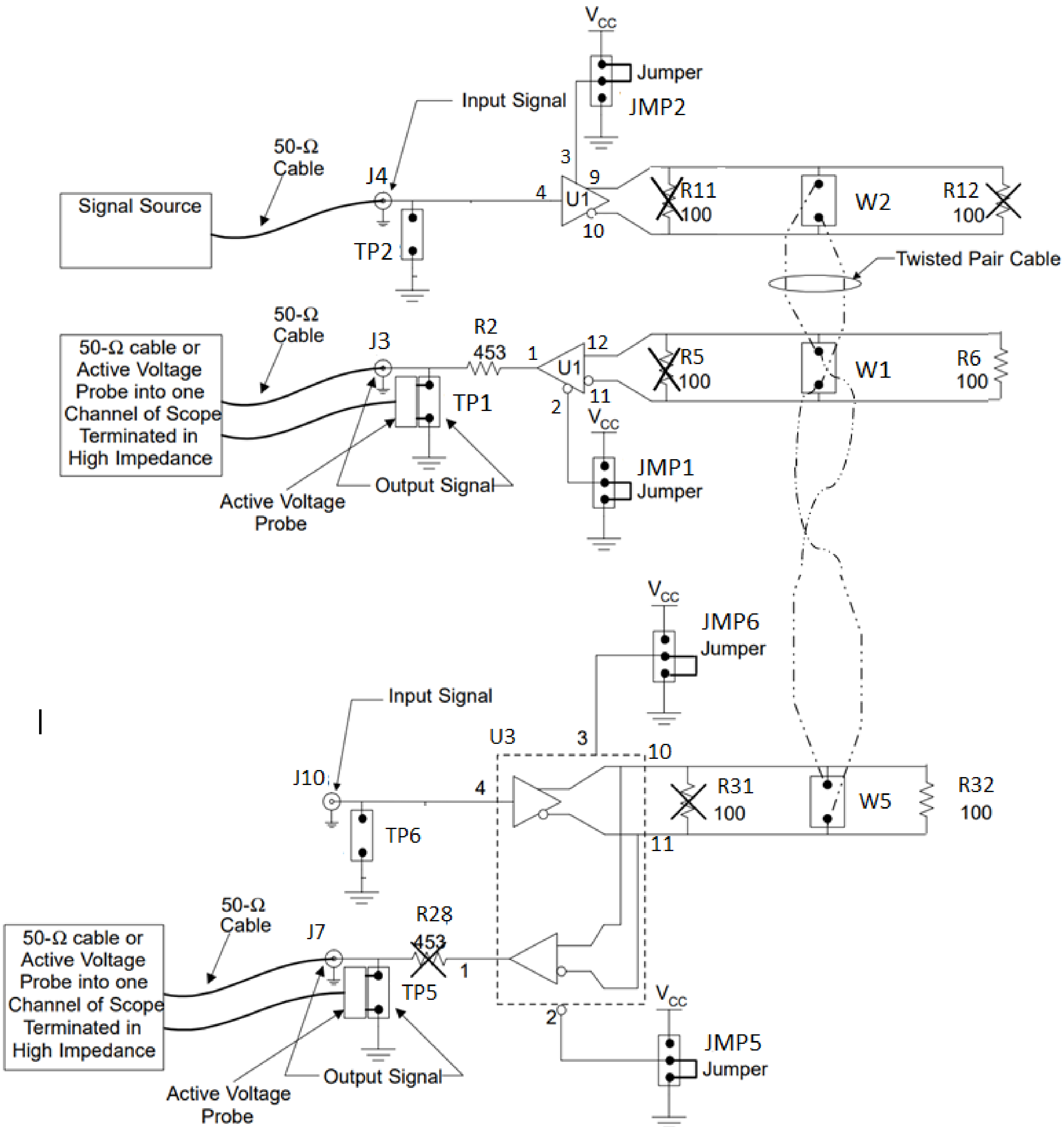


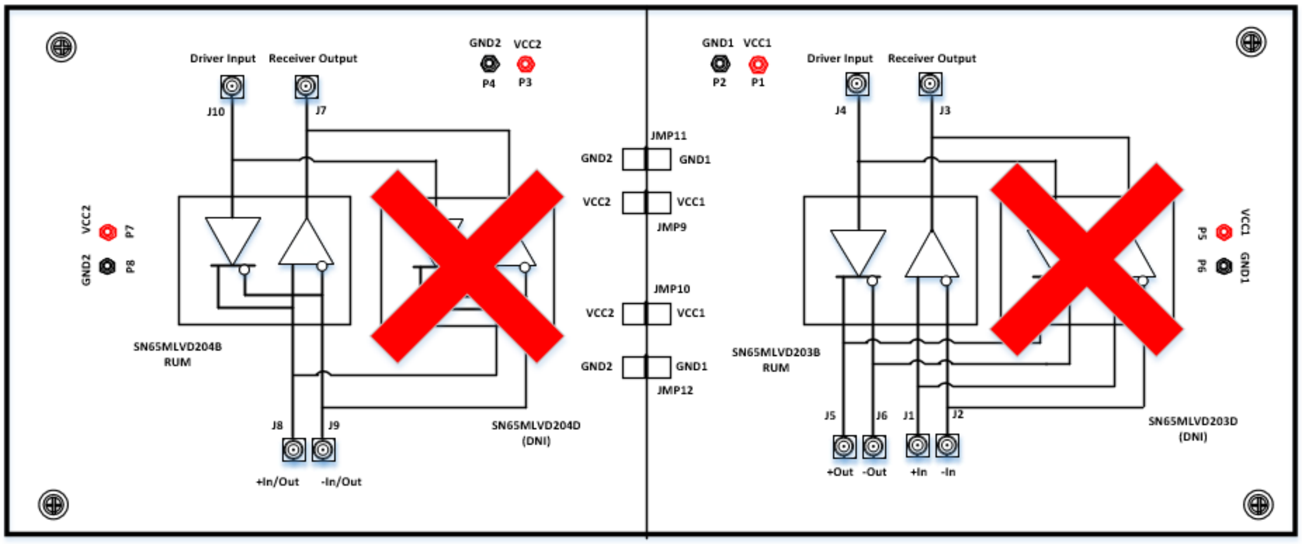
Figure 11. Two-Node Multipoint Transmission

3 Block Diagram, Schematic, and PCB Construction

This chapter contains the bill of materials, schematics, board layout of the M-LVDS, and describes the printed-circuit board.

3.1 Block Diagram

This section shows the block diagram for this EVM.



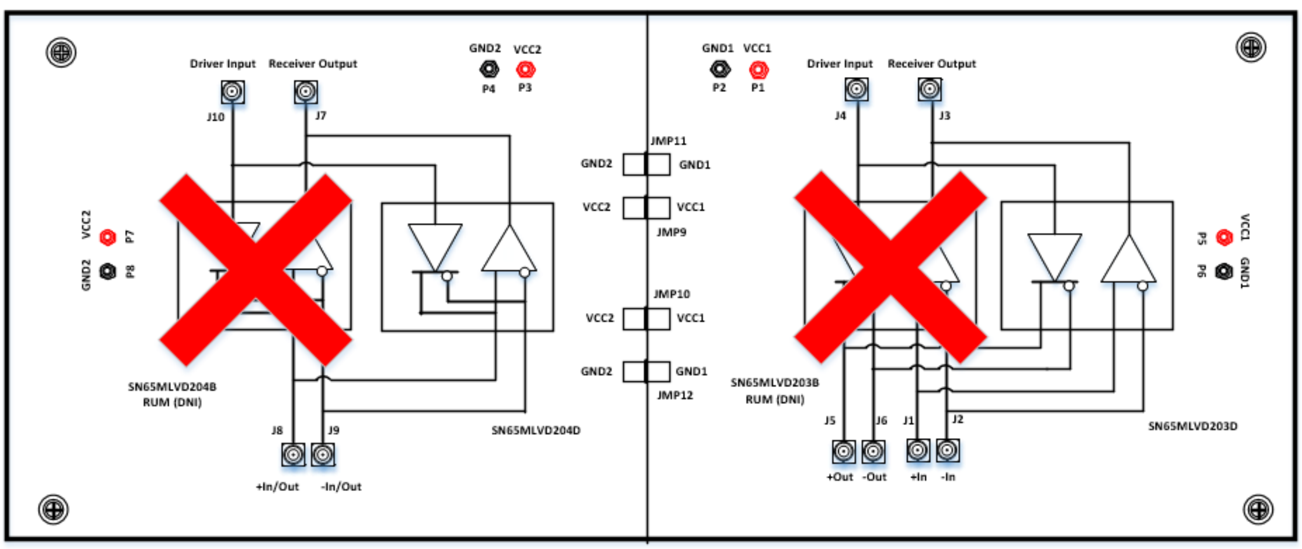


Figure 12. Block Diagram

3.2 Schematic

This section contains the EVM schematic.

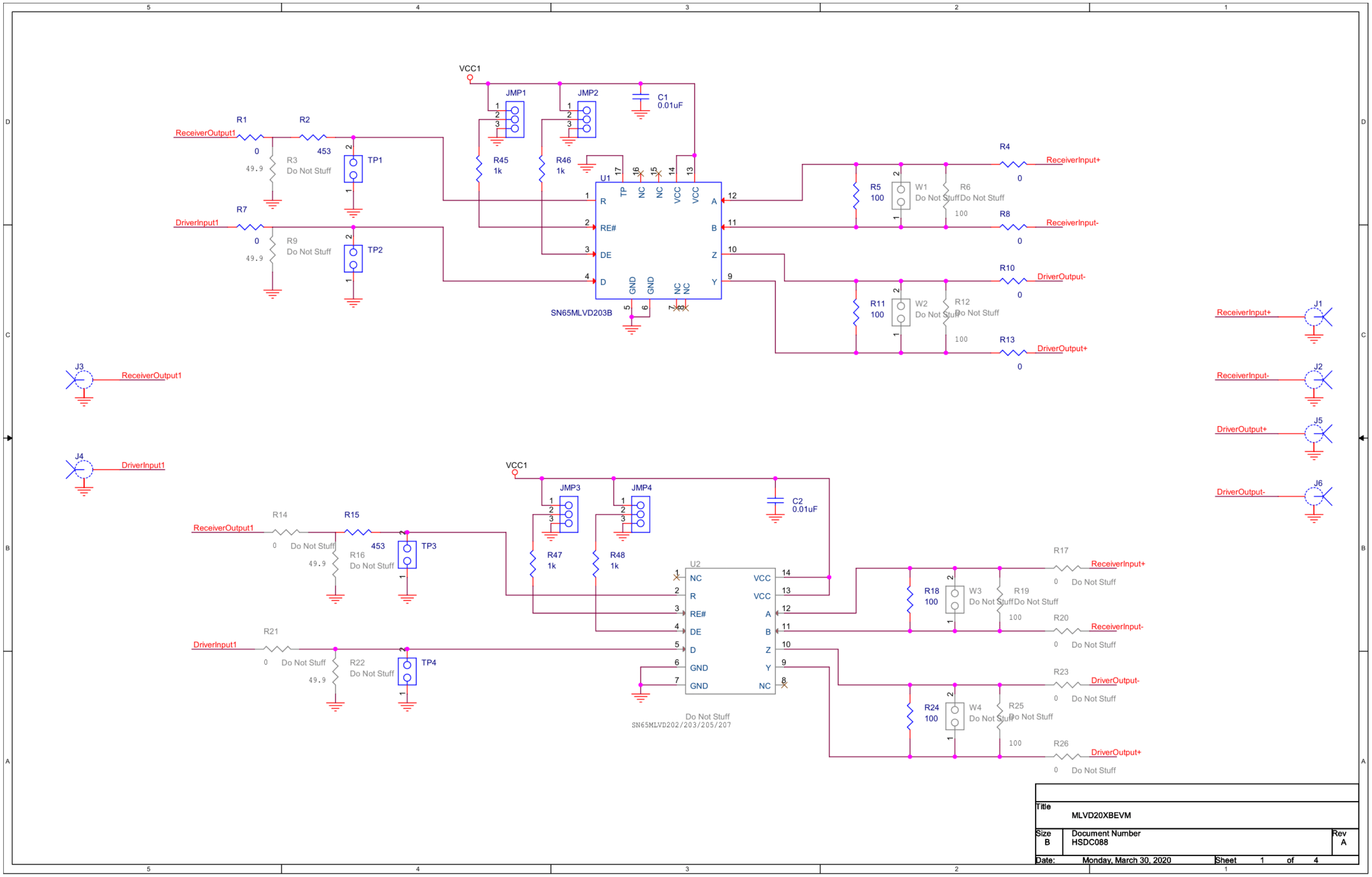


Figure 13. M-LVDS EVM Schematic: Full-Duplex Transceiver

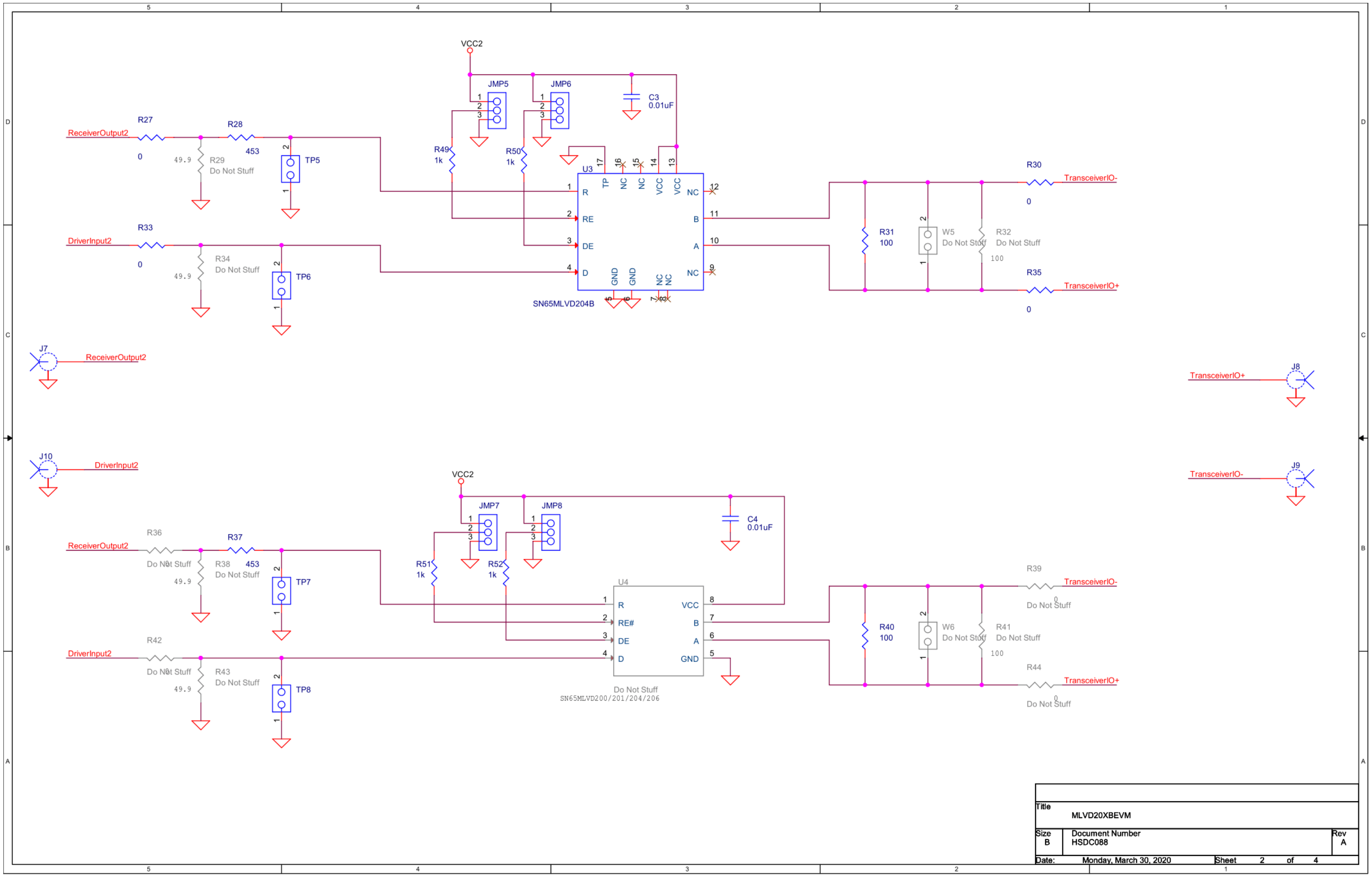


Figure 14. M-LVDS EVM Schematic: Half-Duplex Transceiver

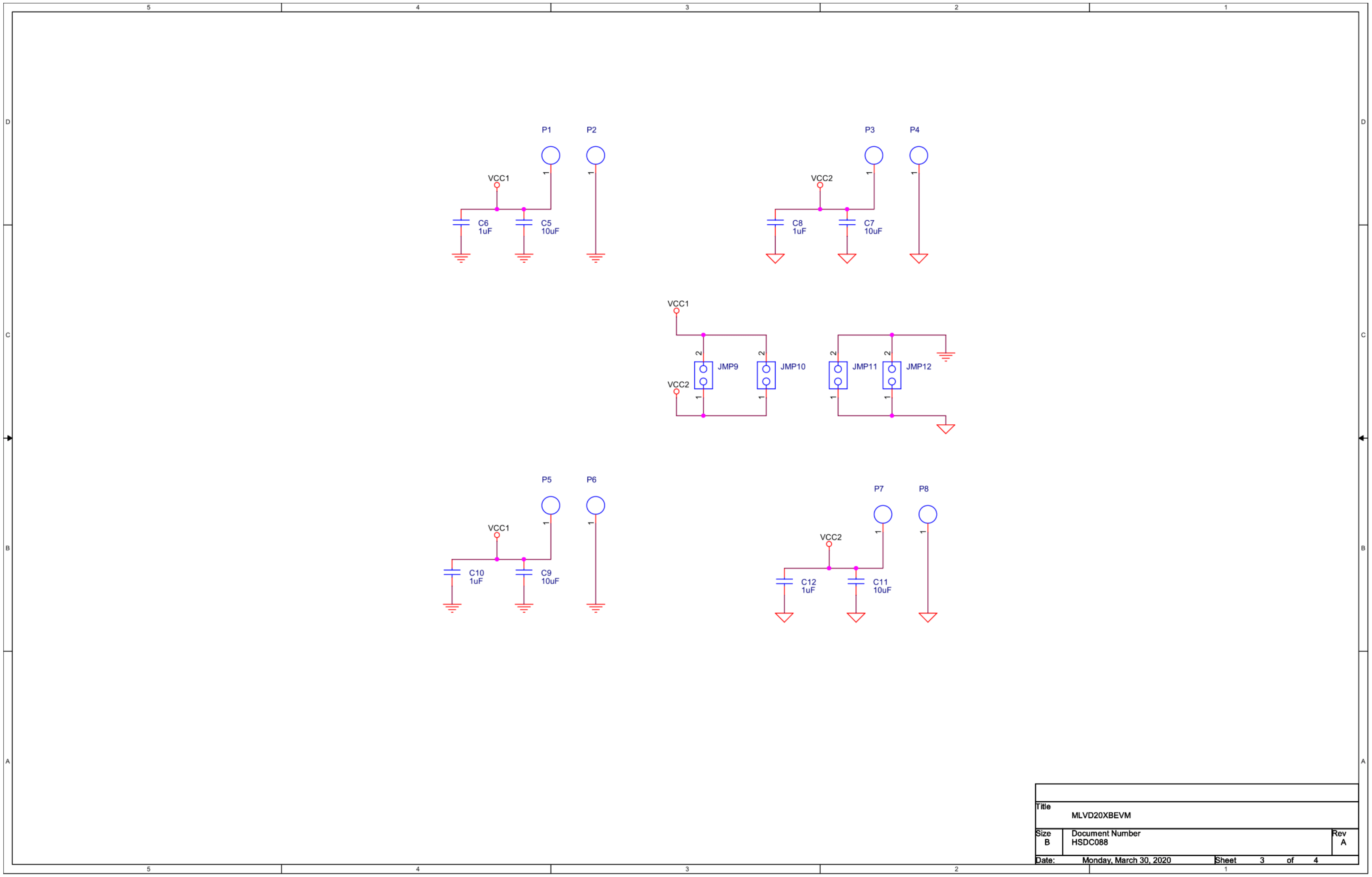


Figure 15. M-LVDS EVM Schematic: Power

3.3 PCB Construction

Information in this section was obtained from the following source:

- *Electromagnetic Compatibility Printed Circuit Board and Electronic Module Design*, VEC workshop, Violette Engineering Corporation.

Characteristic impedance is the ratio of voltage to current in a transmission line wave traveling in one direction. This characteristic impedance is the value that is matched with our termination resistors so as to reduce reflections. This reduction in reflections improves signal to noise ratio on the line and reduces EMI caused by common mode voltages and spikes.

Two typical approaches are used for controlled impedance in printed-circuit board construction, microstrip and stripline. Microstrip construction is shown in Figure 16. The characteristic impedance of a microstrip trace on a printed-circuit board is approximated by:

$$Z_O = \frac{60}{\sqrt{0.475\varepsilon r + 0.67}} \times \ln \frac{4h}{0.67(0.8\ W + t)} \quad (1)$$

where εr is the permeability of the board material, h is the distance between the ground plane and the signal trace, W is the trace width, and t is the thickness of the trace. The differential impedance for a two microstrip traces can be approximated as follows with S being the distance between two microstrip traces:

$$Z_{DIFF} = 2 \times Z_O \times \left(1 - 0.48e^{-0.96s/h}\right) \quad (2)$$

Stripline construction is also shown in Figure 16, the signal lines should be centered between the ground planes. The characteristic impedance of a stripline trace in a printed-circuit board is approximated by:

$$Z_O = \frac{60}{\sqrt{\varepsilon r}} \times \ln \frac{4h}{0.67\pi(0.8\ W + t)} \quad (3)$$

where εr is the permeability of the board material, h is the distance between the ground plane and the signal trace, W is the trace width, and t is the thickness of the trace. The differential impedance for a two stripline traces can be approximated as follows with S being the distance between two stripline traces:

$$Z_{DIFF} = 2 \times Z_O \times \left(1 - 0.37e^{-2.9s/h}\right) \quad (4)$$

NOTE: For edge-coupled striplines, the term 0.374 may be replaced with 0.748 for lines which are closely coupled (S < 12 mils, or 0,3 mm).

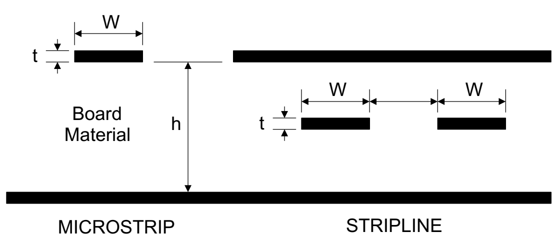


Figure 16. Trace Configurations in Printed-Circuit Boards

Stripline construction is the preferred configuration for differential signaling. This configuration reduces radiated emissions from circuit board traces due to better control of the lines of flux. The additional ground plane also allows for better control of impedance on the traces.

It can be seen from the functions and physical construction parameters that careful consideration must be given to these parameters for a robust board design. For instance it is not uncommon for εr to vary 10% across one board, affecting skew. This is a good reason to keep differential lines close. Other factors to keep in mind when doing a printed-circuit layout for transmission lines are as follows:

1. Differences in electrical length translate into skew.
2. Careful attention to dimensions, length and spacing help to insure isolation between differential pairs.
3. Where possible use *ideal interconnects*, point-to-point with no loads or branches. This keeps the impedance more uniform from end to end and reduce reflections on the line.

4. Discontinuities on the line, vias, pads, test points will:
   - Reduce characteristic impedance
   - Increase the prop delay, and rise-time degradation
   - Increase signal transition time
5. Prioritize signals and avoid turns in critical signals. Turns can cause impedance discontinuities.
6. Within a pair of traces, the distance between the traces should be minimized to maintain common-mode rejection of the receivers. Differential transmission works best when both lines of the pair are kept as identical as possible.

Table 4 shows the layer stack up of the EVM with the defined trace widths for the controlled impedance etch runs using microstrip construction.

Table 4. EVM Layer Stack Up

Material Type: FR 406	Layer No.	Layer Type	Thickness (mils)	Copper Weight	Differential Model			Single-Ended Model	
					Line Width (mils)	Spacing (mils)	Impedance (Ω)	Line Width (mils)	Impedance (Ω)
	1	Signal	0.0006	0.5 oz (start)	0.027	0.23	100	0.042	50
PREPREG			0.025						
	2	Plane	0.0012	1					
CORE			0.004						
	3	Plane	0.0012	1					
PREPREG			0.025						
	4	Signal	0.0006	0.5 oz (start)	0.027	0.23	100	0.042	50

3.4 *Related Documentation From Texas Instruments and Others*

1. *Introduction to M-LVDS* (SLLA108)
2. *LVDS Designer's Notes* (SLLA014A).
3. *Reducing EMI With Low Voltage Differential Signaling* (SLLA030B).
4. *Interface Circuits for TIA/EIA−644 (LVDS)* (SLLA038B).
5. *Transmission at 200 Mpbs in VME Card Cage Using LVDM* (SLLA088).
6. *LVDS Multidrop Connections* (literature number SLLA054).
7. *SN65MLVD20x data sheets, Multipoint-LVDS Line Drivers and Receivers,* (SLLS573 and SLLS558)
8. *Electromagnetic Compatibility Printed Circuit Board and Electronic Module Design*, VEC workshop, Violette Engineering Corporation.

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