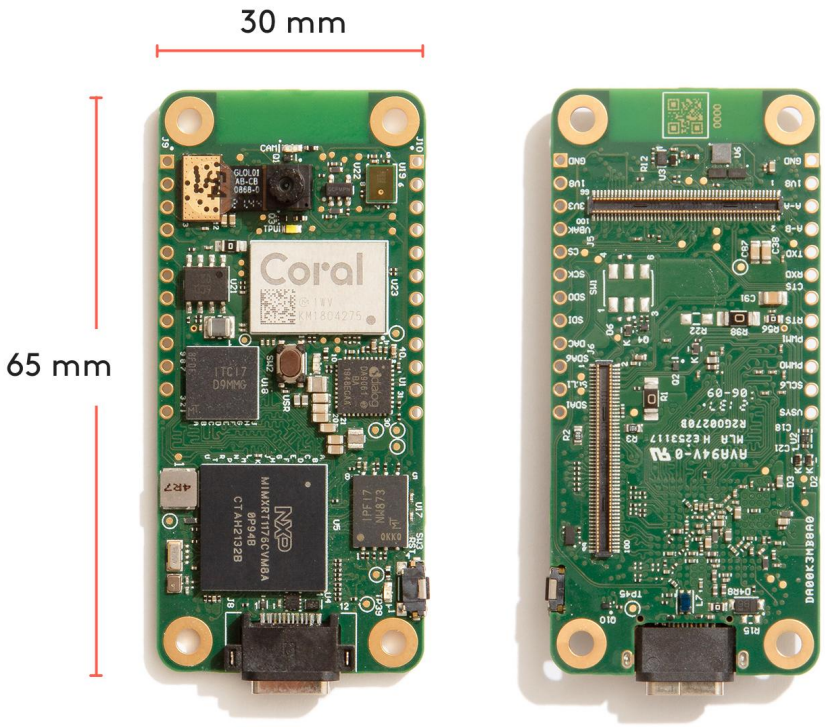
Coral

Dev Board Micro datasheet

Version 1.0

Features

- NXP i.MX RT1176 MCU
  - ARM Cortex-M7 @ 800 MHz
  - ARM Cortex-M4 @ 400 MHz
- Coral Edge TPU ML accelerator
  - 4 TOPS peak performance (int8)
- 128 MiB NAND flash memory
- 64 MB SDRAM
- On-board color camera (324 x 324 px)
  - 2-lane MIPI CSI also available for add-on boards
- On-board PDM microphone
  - Three unused PDM lanes also available for add-on boards
- 24 GPIO header pins
- High-density connectors for add-on boards
  - Coral Wireless Add-on and Coral PoE Add-on sold separately



Description

The Coral Dev Board Micro is a microcontroller board with a dual-core MCU, Coral Edge TPU, camera, and microphone. With this board, you can build low-power systems with fast on-device inferencing for vision and audio ML applications. You can also expand the hardware with custom add-on boards using the high-density board-to-board connectors.

The Edge TPU is a small ASIC designed by Google that accelerates TensorFlow Lite models in a power efficient manner. One Edge TPU is capable of performing 4 trillion operations per second (4 TOPS). This on-device ML processing reduces latency, increases data privacy, and removes the need for a constant internet connection.

Ordering information

Part number	Description
G650-07968-01	Coral Dev Board Micro

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1 System components

Table 1. Dev Board Micro components and features

Feature	Details
NXP i.MX RT1176 MCU	
ARM Cortex-M7	• 800 MHz • 32 KB L1 instruction cache • 32 KB L1 data cache • Floating Point Unit (FPU) with single-precision and double-precision support of Armv7-M architecture FPv5 • Supports TensorFlow Lite for Microcontrollers
ARM Cortex-M4	• 400 MHz • 16 KB instruction cache • 16 KB data cache • Single-precision FPU defined by Armv7-M architecture FPv4-SP • Supports TensorFlow Lite for Microcontrollers

Memory	• 2 MB SRAM:
	  ○ 512 KB of TCM for Cortex-M7
	  ○ 256 KB of TCM for Cortex-M4
	  ○ 1.25 MB OCRAM
	• 4 KB secure always-on RAM
	• 256 KB boot ROM

Secure element	
NXP A71CH	• Cryptographic device authentication • Secure credentials provisioning and storage
ML accelerator	
Coral Edge TPU coprocessor	• High performance inferencing for TensorFlow Lite models • 4 trillion operations per second (TOPS) • USB 2.0 interface with the RT1176 MCU
On-board sensors	
Camera	• Himax HM01B0 CMOS sensor • 324 x 324 px native resolution, or QVGA (320 x 240) • 110° diagonal FOV • *ƒ*/2.0 focal ratio • Fixed focus
Microphone	• Mono microphone (PDM)
Memory and storage	
Random access memory (SDRAM)	• 64 MB
Flash memory (NAND)	• 128 MiB

Hardware connections	
GPIO headers	• 2x 12-pin through-hole interface • GPIO, PWM, UART, I2C, SPI, DAC, ADC, GND, 3V3, 1V8, and VSYS
Board-to-board connectors	• 2x 100-pin connectors (Hirose DF40C-100DP-0.4V(51)) ○ Provides various I/O from the MCU • Supports Coral Wireless Add-on board (sold separately) • Supports Coral PoE Add-on board (sold separately)
USB-C plug	• Board power and USB2 data
User interface	

LEDs	• 4 on-board LEDs:
	  ○ Green LED that indicates camera activity
	  ○ Green LED that's user programmable
	  ○ Orange LED that indicates board operating status
	  ○ White LED that indicates Edge TPU operating status

Switches	• 2 switch buttons:
	  ○ Reset button for the MCU
	  ○ User programmable button for short presses; also power cycles the board with a long press

1.1 Block diagram

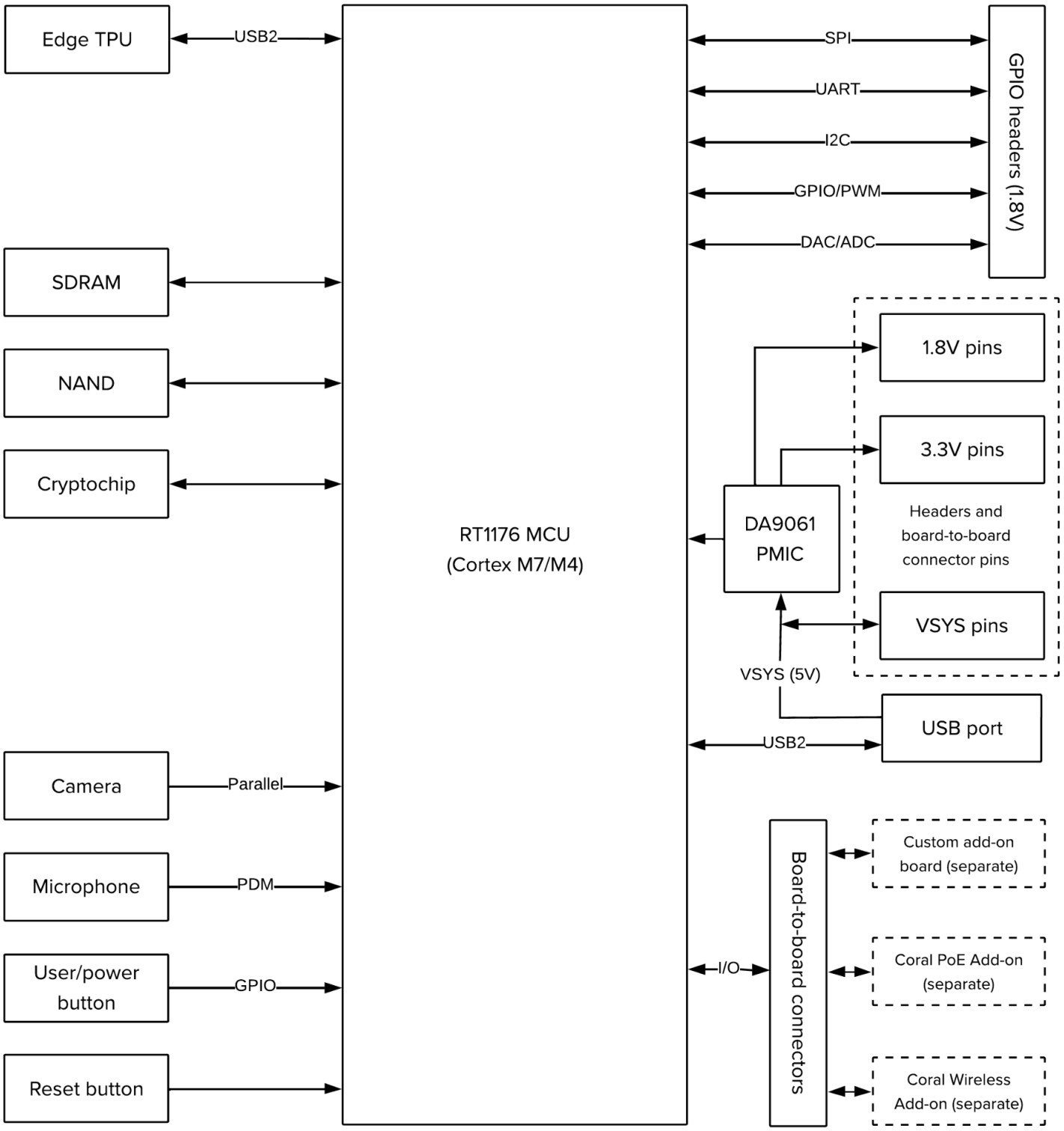

Figure 1. Dev Board Micro functional block diagram

2 Mechanical dimensions

Table 2. Physical specifications

Measurement	Value
Size	65.0 × 30.0 × 6.8 mm
Weight	10.4 g

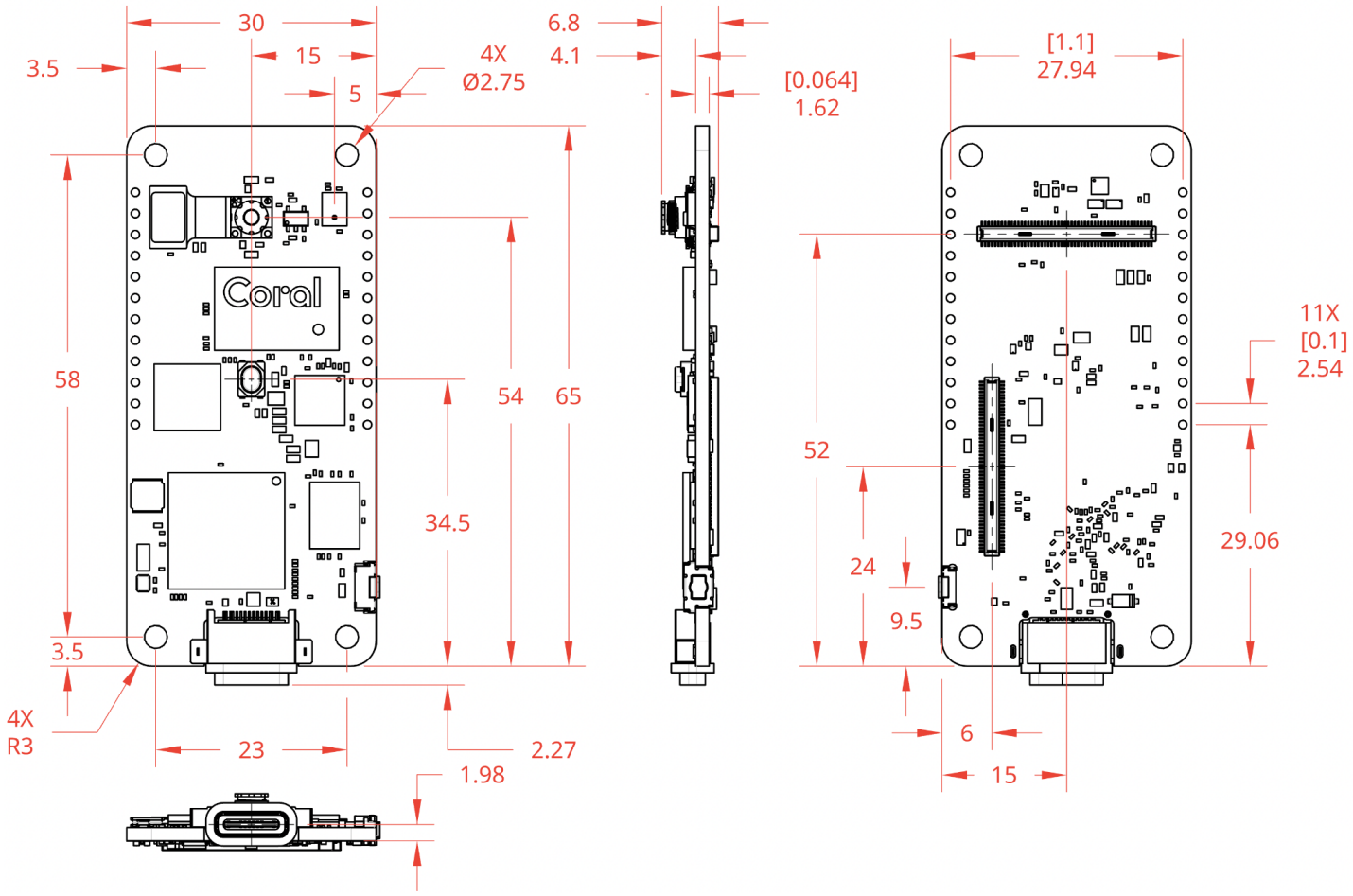

Figure 2. Dev Board Micro dimensions

3 Electrical specifications

3.1 Recommended operating conditions

Table 3. Board operating conditions

Parameter	Min	Typical	Max
Board supply voltage (VSYS)	4.5 V	5 V	5.5 V
Output voltage (VDD_3V3)	3.0 V	3.3 V	3.6 V
Output voltage (VDD_1V8)	1.62 V	1.8 V	1.98 V
RTC supply voltage (VDD_COIN_3V)	2.4 V	3.0 V	3.6 V
GPIO voltage	-0.5 V	1.8 V	2.1 V
Operating temperature	0 °C	–	50 °C
Storage temperature	-30 °C	–	85 °C

Typical operation is based on a 5 V / 2 A power supply via USB. For more details, see section 6.1 Power supply.

Caution: The board can become hot during operation and might burn you if touched. If using a case, the board might require cooling to maintain proper operating temperatures. You must validate safe operation before you deploy.

Warning: Do not connect devices to the voltage rails (VSYS, VDD_3V3, VDD_1V8) that draw significant power. Doing so can exceed the board's ability to supply power and might cause the board to malfunction or overheat, possibly causing fire and serious injury. For details about available power on each rail, consult the Dev Board Micro schematic (table 20).

3.2 Logic threshold levels

Table 4. Digital I/O logic thresholds

Parameter	Output		Input	
	Low-level max (V_{OL})	High-level min (V_{OH})	Low-level max (V_{IL})	High-level min (V_{IH})
GPIO pins	0.54 V	1. 3 V	0.45 V	1.35 V

Note: There is considerable variation in capability between I/O banks on the RT1176 MCU, so only the worst case numbers are provided in table 4. For complete details on I/O drive strengths, refer to the RT1176 datasheet.

When operating within the voltage thresholds in table 4, each I/O pin supports a **maximum current of 6 mA**, except for the DAC pin, which can supply a maximum current of 1 mA. Some signals that are available only through the board-to-board connectors and belong to the GPIO_SNVS domain are limited to 170 µA drive strength.

Warning: If you exceed the max I/O pin current, you can damage the board, possibly causing fire and serious injury.

3.3 Power consumption

The power consumed by the Dev Board Micro depends on a variety of application behaviors, but most importantly, the extent to which the Edge TPU is being used. Typical test scenarios when the Edge TPU is active show average power peaks around 3 W.

Beware that, depending on the type of ML model you're using, the Edge TPU can cause significant spikes in current draw.

For more details about the Edge TPU power consumption, see the Coral Accelerator Module datasheet.

4 Hardware interfaces

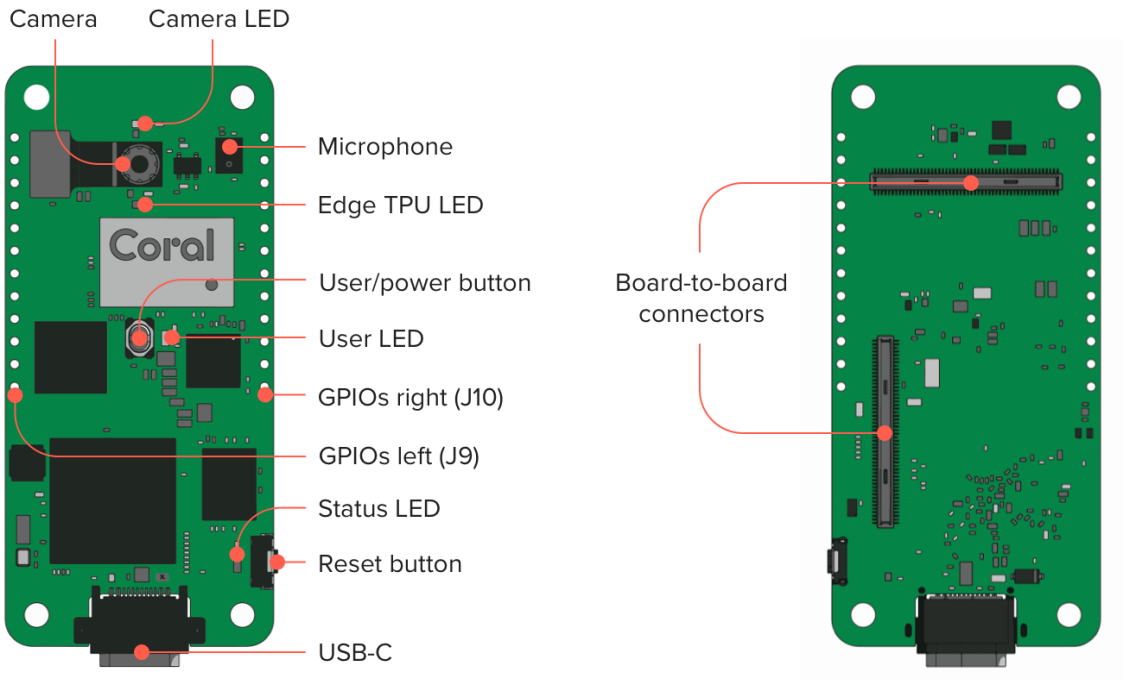

Figure 3. User interface and peripheral components

4.1 Buttons

The Dev Board Micro has two tactile switch buttons:

- **User button / Power cycle (USR):** Programmable for application behaviors with a short press (active low). If held for 7 seconds, it power-cycles the board. If held while booting, it enables Serial Downloader mode.
- **Reset button (RST):** Resets the MCU.

4.2 USB-C port

There is one USB-C port (USB 2.0) that provides board power and data I/O with a computer.

You can access the serial console through USB while FreeRTOS is running (the connection is lost during resets). You can instead access the serial console with the UART pins on the GPIO header and maintain the connection during resets.

4.3 LEDs

All LEDs are programmable, but they have some default behaviors (except the User LED) as described in table 5.

Table 5. Description of the on-board LEDs (see figure 3 for LED locations)

Name	Color	Description
Camera	Green	Indicates camera activity. By default, it is on during image capture, for a minimum of 500 ms.*
TPU	White	Indicates Edge TPU status. By default, it is on while the Edge TPU is powered. It is programmable, but only while the Edge TPU is powered.
User	Green	Programmable. Off by default.
Status	Orange	Indicates board operating status. By default, it turns on briefly when the board boots from flash and it is programmable.

* The Camera LED gives people awareness that images are being captured by an image sensor for storage, processing, and/or transmission. We strongly recommend this LED behavior remain unchanged and always be visible to users.

4.4 Camera

The Dev Board Micro has a low-profile camera module:

- Himax HM01B0 CMOS sensor
- 324 x 324 px native resolution, or QVGA (320 x 240 px)
- 110° diagonal FOV
- *ƒ*/2.0 focal ratio
- Fixed focus

There is also one 2-lane MIPI CSI interface available through the board-to-board connectors for add-on boards.

4.5 Microphone

The Dev Board Micro has one on-board digital PDM microphone (left channel).

There are also 3 unused PDM lanes available through the board-to-board connectors for add-on boards.

4.6 GPIO headers

Each I/O pin on the two 12-pin headers supports a max current of 6 mA when operating with 1.8 V, except for the DAC pin, which must be treated differently and can supply a maximum current of 1 mA. However, drive strengths may be lower and vary between pins. For information about voltage levels and logic thresholds, see section 3 Electrical specifications.

Once FreeRTOS is booted, all I/O pins are set to a high-Z (floating) state, with two exceptions: The I2C pins default to high, and the UART6_TX and UART6_RX lines are configured for serial port communication so their states vary based on serial port activity. During reset and boot-up, all pin states may change. If enabled, internal pull-ups and pull-downs are typically 35 kOhms (for more detail, see the RT1176 datasheet).

Figure 4 shows the primary function for each pin, along with the MCU pin name, and the name you can use to address each pin either as a GPIO with the coralmicro library or as a digital/analog pin with Arduino.

> **Note:** UART6_TX and UART6_RX are configured for serial port communication and should not be used for other purposes.

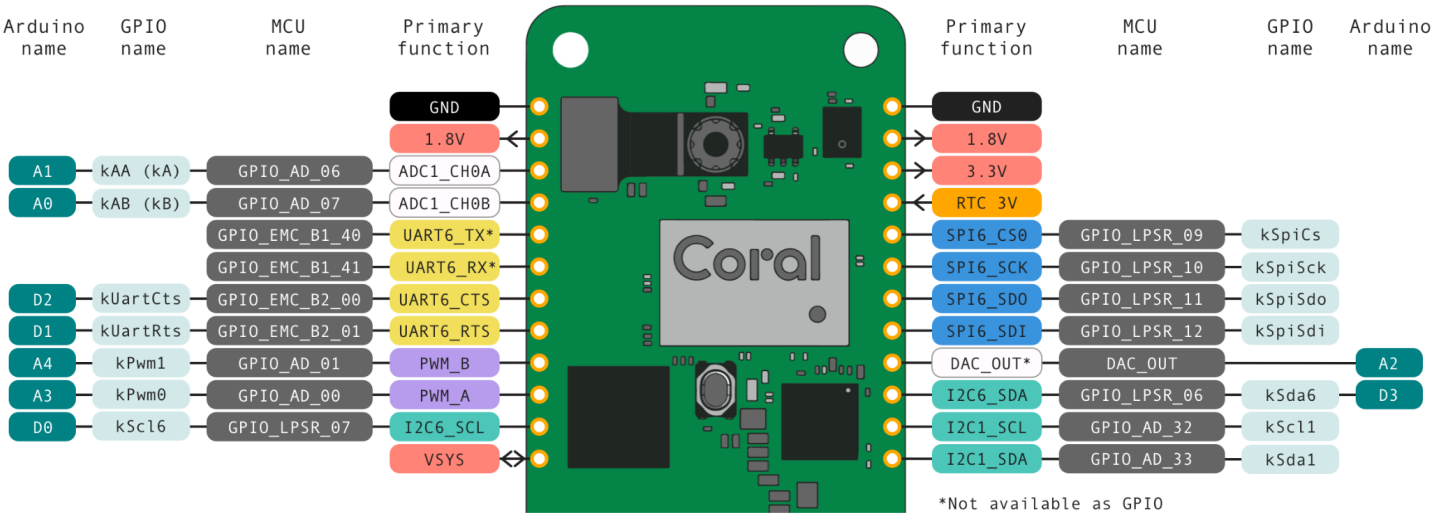

Figure 4. Pin layout and names for the GPIO headers

> **Note:** Header pins are not included. For compatibility with Coral cases, solder the header pins facing down.

4.7 Board-to-board connectors

The Dev Board Micro includes high-density board to board connectors on the bottom of the board (indicated in figure 3), allowing you to connect add-on hardware such as the Coral Wireless Add-on board (sold separately), the Coral PoE Add-on board (sold separately), or other custom add-on hardware.

For details about designing add-on hardware, see section 7 Add-on board developer guide.

5 Peripheral interfaces

The following interfaces are available through the board-to-board connectors ("B2B pins") and, in some cases, also through the GPIO headers ("HDR pins").

5.1 Ethernet

Supports 10/100 Mbps Ethernet/IEEE 802.3 networks via RGMII lanes in the board-to-board connectors. Requires an Ethernet PHY provided by an add-on board.

Table 6. Ethernet pins (all these pins are used by the Coral PoE Add-on)

MCU name	Net name	Type	B2B pin	Voltage	Description
GPIO_DISP_B1_00	ENET_RGMII_RX_EN	Input	J6:76	1.8 V	RGMII receive from PHY.
GPIO_DISP_B1_01	ENET_RGMII_RXC	Input	J6:78	1.8 V	RGMII receive from PHY.
GPIO_DISP_B1_02	ENET_RGMII_RXD0	Input	J6:70	1.8 V	RGMII receive from PHY.
GPIO_DISP_B1_03	ENET_RGMII_RXD1	Input	J6:68	1.8 V	RGMII receive from PHY.
GPIO_DISP_B1_04	ENET_RGMII_RXD2	Input	J6:66	1.8 V	RGMII receive from PHY.
GPIO_DISP_B1_05	ENET_RGMII_RXD3	Input	J6:72	1.8 V	RGMII receive from PHY.
GPIO_DISP_B1_06	ENET_RGMII_TXD3	Output	J6:55	1.8 V	RGMII transmit to PHY. Not for general use.*
GPIO_DISP_B1_07	ENET_RGMII_TXD2	Output	J6:57	1.8 V	RGMII transmit to PHY. Not for general use.*
GPIO_DISP_B1_08	ENET_RGMII_TXD1	Output	J6:59	1.8 V	RGMII transmit to PHY. Not for general use.*
GPIO_DISP_B1_09	ENET_RGMII_TXD0	Output	J6:61	1.8 V	RGMII transmit to PHY. Not for general use.*
GPIO_DISP_B1_10	ENET_RGMII_TX_EN	Output	J6:63	1.8 V	RGMII transmit to PHY. Not for general use.*
GPIO_DISP_B1_11	ENET_RGMII_TXC	Output	J6:65	1.8 V	RGMII transmit to PHY. Not for general use.*
GPIO_EMC_B2_19	ENET_RGMII_MDC	Output	J6:44	1.8 V	RGMII clock for PHY.
GPIO_EMC_B2_20	ENET_RGMII_MDIO	I/O	J6:46	1.8 V	RGMII MDIO data for PHY.
GPIO_EMC_B2_03	ETHPHY_RST_B	Output	J6:42	1.8 V	PHY reset.
GPIO_EMC_B2_02	RGMII1_PHY_INTB	Input	J6:40	1.8 V	PHY interrupt.

* GPIO_DISP_B1_06 through 11 are not for general use because they require special consideration to avoid driving these pins at boot. Failure to handle them properly may cause boot failure.

5.2 SDIO

Table 7. SDIO pins

MCU name	Net name	Type	B2B pin	Voltage	Description
GPIO_SD_B1_00	WIFI_SDIO_CMD	Output	J5:100	1.8 V	Used by Coral Wireless Add-on.
GPIO_SD_B1_01	WIFI_SDIO_CLK	Input	J5:92	1.8 V	Used by Coral Wireless Add-on.
GPIO_SD_B1_02	WIFI_SDIO_D0	I/O	J5:96	1.8 V	Used by Coral Wireless Add-on.
GPIO_SD_B1_03	WIFI_SDIO_D1	I/O	J5:94	1.8 V	Used by Coral Wireless Add-on.
GPIO_SD_B1_04	WIFI_SDIO_D2	I/O	J5:85	1.8 V	Used by Coral Wireless Add-on.
GPIO_SD_B1_05	WIFI_SDIO_D3	I/O	J5:98	1.8 V	Used by Coral Wireless Add-on.
GPIO_SD_B2_00	USDHC2_DATA3	I/O	J5:71	1.8 V	uSDHC data bit 3.
GPIO_SD_B2_01	USDHC2_DATA2	I/O	J5:75	1.8 V	uSDHC data bit 2.
GPIO_SD_B2_02	USDHC2_DATA1	I/O	J5:73	1.8 V	uSDHC data bit 1.
GPIO_SD_B2_03	USDHC2_DATA0	I/O	J5:77	1.8 V	uSDHC data bit 0.
GPIO_SD_B2_04	USDHC2_CLK	Output	J5:79	1.8 V	uSDHC serial clock.
GPIO_SD_B2_05	USDHC2_CMD	Output	J5:81	1.8 V	uSDHC command line.

5.3 CSI camera

One 2-lane MIPI CSI bus with up to 1.5 GHz bit rate clock. Supports 24-bit RGB888/YUV444, CCIR656 video interface, 8-bit YCbCr, YUV or RGB, and 8-bit/10-bit/16-bit/24-bit Bayer data input. Compatible with MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.1.

Note: The CSI channels have not been not tested with real-world applications. They have been tested only for nominal impedance during manufacturing testing.

Table 8. MIPI Camera Serial Interface (CSI) pins

Net name	Type	B2B pin	Voltage	Description
MIPI_CSI_CK_P	Input	J6:92	1.8 V	MIPI CSI clock positive.
MIPI_CSI_CK_N	Input	J6:94	1.8 V	MIPI CSI clock negative.
MIPI_CSI_D0_P	Input	J6:86	1.8 V	MIPI CSI data lane 0 positive.
MIPI_CSI_D0_N	Input	J6:88	1.8 V	MIPI CSI data lane 0 negative.
MIPI_CSI_D1_P	Input	J6:98	1.8 V	MIPI CSI data lane 1 positive.
MIPI_CSI_D1_N	Input	J6:100	1.8 V	MIPI CSI data lane 1 negative.

5.4 DSI display

One 2-lane MIPI DSI bus with up to 1.5 GHz bit rate clock. Conforms to the MIPI D-PHY electrical specifications MIPI Display Serial Interface (DSI) Version 1.1 and D-PHY specification Rev. 1.0 (and also MIPI Display Pixel Interface version 2.0, MIPI Display Bus Interface version 2.0, DSC version 1.0a at protocol layer) for MIPI display port x2 lanes.

Note: The DSI channels are not tested with real-world applications. They are only tested for nominal impedance during manufacturing testing.

Table 9. MIPI Display Serial Interface (DSI) pins

Net name	Type	B2B pin	Voltage	Description
MIPI_DSI_CK_P	Output	J6:85	1.8 V	MIPI DSI clock positive.
MIPI_DSI_CK_N	Output	J6:87	1.8 V	MIPI DSI clock negative.
MIPI_DSI_D0_P	Output	J6:79	1.8 V	MIPI DSI data lane 0 positive.
MIPI_DSI_D0_N	Output	J6:81	1.8 V	MIPI DSI data lane 0 negative.
MIPI_DSI_D1_P	Output	J6:91	1.8 V	MIPI DSI data lane 1 positive.
MIPI_DSI_D1_N	Output	J6:93	1.8 V	MIPI DSI data lane 1 negative.

5.5 PDM audio

Table 10. Pulse density modulation (PDM) pins

MCU name	Net name	Type	B2B pin	Voltage	Description
GPIO_LPSR_00	MIC_CLK	Output	J5:97	1.8 V	Used by on-board microphone.
GPIO_LPSR_01	DMIC_DATA0	Input	J5:45	1.8 V	Used by on-board microphone.
GPIO_LPSR_13	DMIC_DATA1	Input	J5:43	1.8 V	Shared with JTAG_MUX_MOD.
GPIO_LPSR_14	DMIC_DATA2	Input	J5:41	1.8 V	Shared with JTAG_TCK.
GPIO_LPSR_15	DMIC_DATA3	Input	J5:39	1.8 V	Shared with JTAG_TMS.

5.6 SAI audio

Table 11. Serial audio interface (SAI) pins

MCU name	Net name	Type	B2B pin	Voltage	Description
GPIO_EMC_B2_04	SAI2_MCLK	I/O	J5:66	1.8 V	Audio master clock.
GPIO_EMC_B2_05	SAI2_RX_SYNC	I/O	J5:62	1.8 V	Receive frame sync.
GPIO_EMC_B2_06	SAI2_RX_BCLK	Output	J5:42	1.8 V	Receive bit clock.
GPIO_EMC_B2_07	SAI2_RX_DATA	Input	J5:68	1.8 V	Receive channel.
GPIO_EMC_B2_08	SAI2_TX_DATA	Output	J5:53	1.8 V	Transmit channel.
GPIO_EMC_B2_09	SAI2_TX_BCLK	Output	J5:64	1.8 V	Transmit bit clock.
GPIO_EMC_B2_10	SAI2_TX_SYNC	I/O	J5:40	1.8 V	Transmit frame sync.

5.7 ADC

Table 12. General purpose 12-bit analog-digital-converters (ADC) pins

MCU name	Net name	Type	B2B pin	HDR pin	Voltage	Description
GPIO_AD_11	ADC1_CH2B	Input	J5:6	-	1.8 V	
GPIO_AD_06	ADC1_CH0A	Input	J5:10	J9:3	1.8 V	Mux to CAN1_RX.
GPIO_AD_07	ADC1_CH0B	Input	J5:14	J9:4	1.8 V	Mux to CAN1_TX.

5.8 DAC

Table 13. General purpose 12-bit digital-analog-converter (DAC) pins

MCU/Net name	Type	B2B pin	HDR pin	Voltage	Description
DAC_OUT	Output	J5:95	J10:9	1.8 V	

5.9 I2C

Table 14. Inter-integrated circuit (I2C) pins

MCU name	Name	Type	B2B pin	HDR pin	Voltage	Description
GPIO_AD_32	I2C1_SCL	I/O	J5:51	J10:11	1.8 V	
GPIO_AD_33	I2C1_SDA	I/O	J5:52	J10:12	1.8 V	
GPIO_LPSR_04	I2C5_SDA	I/O	J5:15	-	1.8 V	Internal I2C bus SDA.
GPIO_LPSR_05	I2C5_SCL	I/O	J5:17	-	1.8 V	Internal I2C bus SCL.
GPIO_LPSR_06	I2C6_SDA	I/O	J5:72	J10:10	1.8 V	
GPIO_LPSR_07	I2C6_SCL	I/O	J5:35	J9:11	1.8 V	

5.10 UART

Table 15. Universal asynchronous receiver/transmitter (UART) pins

MCU name	Net name	Type	B2B pin	HDR pin	Voltage	Description
GPIO_AD_24	LPUART1_TXD	Output	J5:89	-	1.8 V	NC to MCU at boot. To use these pins, drive GPIO_AD_05 high.
GPIO_AD_25	LPUART1_RXD	Input	J5:91	-	1.8 V	
GPIO_DISP_B2_10	LPUART2_TXD	Output	J6:58	-	1.8 V	Used by Coral Wireless Add-on.
GPIO_DISP_B2_11	LPUART2_RXD	Input	J6:60	-	1.8 V	Used by Coral Wireless Add-on.
GPIO_DISP_B2_12	LPUART2_CTS_B	Input	J6:56	-	1.8 V	Used by Coral Wireless Add-on.
GPIO_DISP_B2_13	LPUART2_RTS_B	Output	J6:54	-	1.8 V	Used by Coral Wireless Add-on.
GPIO_EMC_B2_00	LPUART6_CTS	Input	J5:24	J9:7	1.8 V	
GPIO_EMC_B2_01	LPUART6_RTS	Output	J5:47	J9:8	1.8 V	
GPIO_EMC_B1_40	LPUART6_TXD	Output	J5:2	J9:5	1.8 V	
GPIO_EMC_B1_41	LPUART6_RXD	Input	J5:22	J9:6	1.8 V	
GPIO_DISP_B2_08	LPUART8_TXD	Output	J6:52	-	1.8 V	
GPIO_DISP_B2_09	LPUART8_RXD	Input	J5:82		1.8 V	

5.11 SPI

Table 16. Serial peripheral interface (SPI) pins

MCU name	Net name	Type	B2B pin	HDR pin	Voltage	Description
GPIO_AD_28	LPSPI1_SCK	Output	J6:69	-	1.8 V	
GPIO_AD_29	LPSPI1_PCS0	Output	J6:71	-	1.8 V	
GPIO_AD_30	LPSPI1_SDO	Output	J6:73	-	1.8 V	
GPIO_AD_31	LPSPI1_SDI	Input	J6:75	-	1.8 V	
GPIO_LPSR_09	LPSPI6_CS0	Output	J5:50	J10:5	1.8 V	
GPIO_LPSR_10	LPSPI6_SCK	Output	J5:48	J10:6	1.8 V	Shared with JTAG_MUX_TRSTB.
GPIO_LPSR_11	LPSPI6_SDO	Output	J5:46	J10:7	1.8 V	Shared with JTAG_MUX_TDO.
GPIO_LPSR_12	LPSPI6_SDI	Input	J5:44	J10:8	1.8 V	Shared with JTAG_MUX_TDI.

5.12 GPIO

Table 17. General purpose input/output (GPIO) pins

MCU name	Net name	Type	B2B pin	Voltage	Description
GPIO_DISP_B2_06	WL_ANT_SEL	Output	J5:88	1.8 V	Used by Coral Wireless Add-on.
GPIO_DISP_B2_07	WL_HOST_WAKE	Input	J5:86	1.8 V	Used by Coral Wireless Add-on.
GPIO_DISP_B2_14	BT_DEV_WAKE	Output	J6:62	1.8 V	Used by Coral Wireless Add-on.
GPIO_DISP_B2_15	BT_HOST_WAKE	Input	J6:50	1.8 V	Used by Coral Wireless Add-on.
GPIO_AD_34	WL_REG_ON	Output	J5:93	1.8 V	Used by Coral Wireless Add-on.
GPIO_AD_35	BT_REG_ON	I/O	J5:87	1.8 V	Used by Coral Wireless Add-on.
GPIO_SNVS_00	USER_BUTTON	I/O	J5:31	1.8 V	
GPIO_SNVS_02	BRD_STAT_LED	I/O	J5:80	1.8 V	
GPIO_SNVS_03	USER_LED	I/O	J5:25	1.8 V	
GPIO_SNVS_04	GPIO_SNVS_04	I/O	J5:58	1.8 V	
GPIO_SNVS_05	CAMERA_INT	I/O	J5:33	1.8 V	
GPIO_SNVS_06	GPIO_SNVS_06	I/O	J5:78	1.8 V	
GPIO_SNVS_07	GPIO_SNVS_07	I/O	J5:34	1.8 V	
GPIO_SNVS_08	GPIO_SNVS_08	I/O	J5:56	1.8 V	
GPIO_SNVS_09	WIFI_POWER_EN	I/O	J5:27	1.8 V	Used by Coral Wireless Add-on.

5.13 PWM

Table 18. Pulse-width modulation (PWM) pins

MCU name	Net name	Type	B2B pin	HDR pin	Voltage	Description
GPIO_AD_00	FLEXPWM1_PWM0_A	Output	J5:9	J9:10	1.8 V	
GPIO_AD_01	FLEXPWM1_PWM0_B	Output	J5:7	J9:9	1.8 V	
GPIO_AD_02	FLEXPWM1_PWM1_A	Output	J5:11	-	1.8 V	Used internally for TPU LED.
GPIO_AD_03	FLEXPWM1_PWM1_B	Output	J5:5	-	1.8 V	
GPIO_AD_26	FLEXPWM2_PWM1_A	Output	J5:3	-	1.8 V	
GPIO_AD_27	FLEXPWM2_PWM1_B	Output	J5:1	-	1.8 V	

5.14 JTAG

Table 19. JTAG debugging pins

MCU name	Net name	Type	B2B pin	HDR pin	Voltage	Description
GPIO_LPSR_10	JTAG_nTRST	Output	J5:48	J10:6 (SPI)	1.8 V	Shared with LPSPI6_SCK.
GPIO_LPSR_11	JTAG_TDO	Output	J5:46	J10:7 (SPI)	1.8 V	Shared with LPSPI6_TDO.
GPIO_LPSR_12	JTAG_TDI	Input	J5:44	J10:8 (SPI)	1.8 V	Shared with LPSPI6_SDI.
GPIO_LPSR_13	JTAG_MOD	Input	J5:43	-	1.8 V	Shared with DMIC_DATA1.
GPIO_LPSR_14	JTAG_TCK	Input	J5:41	-	1.8 V	Shared with DMIC_DATA2.
GPIO_LPSR_15	JTAG_TMS	Input	J5:39	-	1.8 V	Shared with DMIC_DATA3.

6 Board operation

6.1 Power supply

You can power the Dev Board Micro through either the USB-C port or the VSYS pins available on the GPIO header and board-to-board connectors.

The Dev Board Micro requires a DC power supply that can provide 5 V at 2 A. Although applications can operate at lower currents, the Edge TPU can produce significant power spikes during inferencing, so the supply must be able to handle peak current transients.

The power supply is intended to support the Dev Board Micro's power requirements only. If using the Dev Board Micro to control a device that draws significant loads, you should provide that device with a separate power supply. For details about the Dev Board Micro's output voltage rails, refer to section 3.1 Recommended operating conditions.

Caution: If your power supply cannot deliver 5 V at 2 A, the Dev Board Micro might not operate reliably. If powering the board from a computer that can't deliver sufficient power, you should connect the board through a powered USB hub.

Warning: Do not connect more than one power source at a time. For example, do not connect the USB port to a power supply when also delivering power through the Coral PoE Add-on board (or other add-on board) or through the VSYS header. Doing so can degrade the USB power supply's ability to power the board, and can cause damage to the power supply at the VSYS pin, possibly causing fire and serious injury.

6.2 Boot modes

The Dev Board Micro has two primary boot modes: Boot from flash memory or boot the Serial Downloader.

During a normal boot, the Dev Board Micro loads an application from flash memory. To instead boot the Serial Downloader, hold the User button (the button at the center of the board) as the board boots. That is, either tap the Reset button or plug in the board while you hold the User button.

Note: If you start the Serial Downloader by holding the User button as you connect power to the Dev Board Micro, the Status LED remains solid because its line is pin-strapped high. (When booting from flash, the Status LED quickly turns off because the pin changes to an input.) Whereas, if you start the Serial Downloader by holding the User button as you press the Reset button, all pins maintain their prior state, so the Status LED could be either on or off, depending on the application that was running at the time.

You can flash the Dev Board Micro while it's in either boot mode. To flash the board, connect it to your computer via the USB port, and use the Python flashtool provided with the coralmicro source code. For details, see the Dev Board Micro setup guide.

7 Add-on board developer guide

This section provides information to help you build custom hardware ("add-on boards") that attaches to the Coral Dev Board Micro using the board-to-board connectors on the bottom of the board.

7.1 Design files

For help designing add-on boards, refer to the mechanical and electrical documents in table 20.

Table 20. Reference design files

Files	Description
Dev Board Micro schematic	Electrical schematic for the main board
Dev Board Micro models	3D model files for the main board
Add-on board KiCad templates	Design file templates for add-on boards

7.2 Baseboard connectors

The connector layout dimensions are indicated in figure 2, in section 2 Mechanical dimensions.

Table 21 specifies the 100-pin connectors that are compatible with the Dev Board Micro.

Table 21. Dev Board Micro and matching add-on board connectors

Dev Board Micro connector	Add-on board connector
2x 100-position plug Hirose Electric DF40C-100DP-0.4V(51)	2x 100-position receptacle 1.5mm B2B height: Hirose Electric DF40HC-100DS-0.4V(51) 3.0mm B2B height: Hirose Electric DF40HC(3.0)-100DS-0.4V(51)

7.2.1 Connector pinouts

For pinout details, refer to the Dev Board Micro schematic in table 20.

7.3 Component max heights and keepouts

The maximum component height on the bottom is nominally 1 mm, when ignoring the board-to-board connectors. The minimum board-to-board spacing between the Dev Board Micro and any add-on boards is 1.5 mm.

For detailed component heights, see the Dev Board Micro model files in table 20.

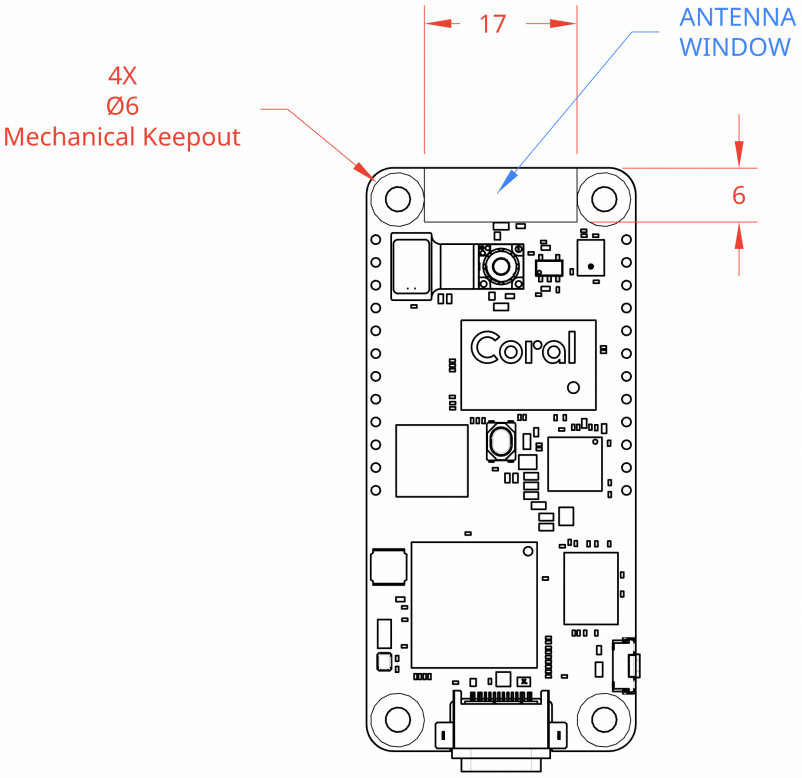

Figure 5. Top view of the Dev Board Micro showing keepout regions for the add-on board antennas

7.4 Trace impedance recommendations

Table 22. Trace impedance recommendations for high-speed signals

Signal group	Impedance	PCB manufacture tolerance (±)
All single-ended signals (Ethernet), unless specified	50 Ohm single-ended	10%
USB differential signals	90 Ohm differential	10%
Differential signals: including Ethernet, MIPI (CSI and DSI)	100 Ohm differential	10%

7.5 MIPI trace length compensation

MIPI signals for the CSI/DSI buses are high-speed signals that require that the total etched trace lengths for each line within a group (the paired clock lanes and four data lanes) be equal to each other. Due to space constraints on the board, the MIPI signal traces lengths are not exactly equal (as indicated in tables 23 and 24). You must incorporate the length difference on your add-on hardware traces, as necessary, such that the trace lengths for each MIPI group match each other.

Table 23. MIPI CSI trace lengths on the board

Name	Etch length		Manhattan length	
	mils	mm	mils	mm
MIPI_CSI_CKP	289.3	7.348	288.8	7.336
MIPI_CSI_CKN	288.8	7.336	288.3	7.323
MIPI_CSI_DP0	289.6	7.356	289.1	7.343
MIPI_CSI_DN0	287.8	7.310	287.3	7.297
MIPI_CSI_DP1	286.7	7.282	286.6	7.280
MIPI_CSI_DN1	287.3	7.297	286.6	7.280

Table 24. MIPI DSI trace lengths on the board

Name	Etch length		Manhattan length	
	mils	mm	mils	mm
MIPI_DSI_CKP	369.7	9.390	275.4	6.995
MIPI_DSI_CKN	369.4	9.383	374.8	9.520
MIPI_DSI_DP0	373.8	9.495	379.5	9.639
MIPI_DSI_DN0	373.5	9.487	379.0	9.627
MIPI_DSI_DP1	370.6	9.413	376.3	9.558
MIPI_DSI_DN1	370.8	9.418	376.3	9.558

7.6 Other recommendations

- When placing a pull-up or pull-down resistor on any signals broken out from the Dev Board Micro, check the Dev Board Micro schematic (table 20) to confirm that pull up/down resistors do not already exist on these signals.

8 Document revisions

Table 25. History of changes to this document

Version	Changes
1.0	Initial release.

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