EV2760-VT-00A

I^2C-Controlled, 1-Cell to 4-Cell, Buck-Boost NVDC Charger with Reverse Source Mode Evaluation Board

DESCRIPTION

The EV2760-VT-00A evaluation board is designed to demonstrate the capabilities of the MP2760, a buck-boost, narrow voltage DC (NVDC) charger IC designed for applications with 1-cell to 4-cell series battery packs.

The MP2760 can accept a wide 4V to 22V operating input voltage (V_{IN}) range to charge the battery and power the load connected on SYS. The device also supplies a wide 3V to 21V voltage at the IN pin in source mode, which is compliant with USB powered device (PD) specifications.

When input power is present, the EV2760-VT-00A charges the battery with a maximum 6A charge current. It can also supply voltage at the input when source mode is enabled. In source mode, the output current (I_{OUT}) is limited to 6A.

The MP2760 is available in a TQFN-30 (4mmx5mm) package.

PERFORMANCE SUMMARY (1)

Specifications are at T_A = 25°C, unless otherwise noted.

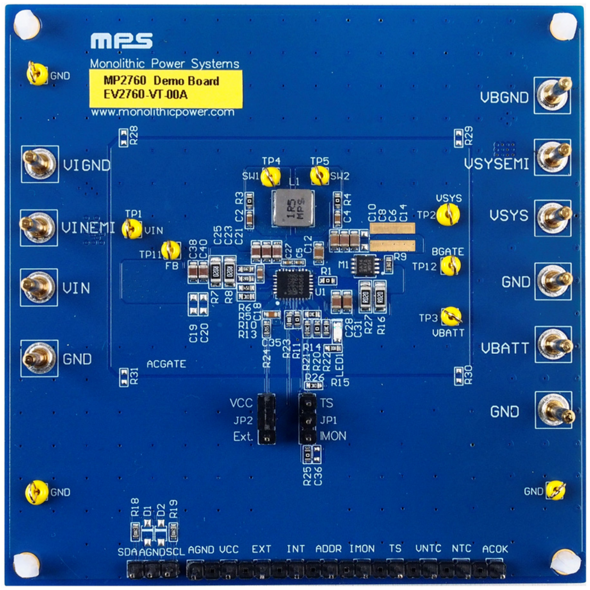
Parameters	Conditions	Value
Input voltage (V_{IN}) range		4V to 22V
Battery charge regulation voltage (V_{BATT_REG})	2 cells	8.4V (I^2C-configurable)
Fast charge current (I_{CC})	V_{IN} = 9V to 22V	2A (I^2C-configurable)
System voltage ($V_{SYS\_MIN\_REG}$)	2 cells	6.5V (I^2C-configurable)
Output voltage in source mode (V_{IN_SRC}) range		3V to 21V
Output voltage in source mode (V_{IN_SRC})		4.98V (I^2C-configurable)
Output current limit in source mode (I_{IN_SRC})		2A (I^2C-configurable)
Charge typical efficiency	V_{IN} = 20V, V_{BATT} = 8V, I_{CC} = 5A	93.49%
Charge peak efficiency	V_{IN} = 12V, V_{BATT} = 8V, I_{CC} = 3A	96%
Source mode typical efficiency	V_{BATT} = 7.4V, V_{IN_SRC} = 20V, I_{IN_SRC} = 1.5A	93.5%
Source mode peak efficiency	V_{BATT} = 8.4V, V_{IN_SRC} = 12V, I_{IN_SRC} =1.5A	96.37%
Switching frequency (f_{SW})		600kHz (I^2C-configurable)

Note:

1) Refer to the MP2760 datasheet for details.

MPL Optimized Performance with MPS Inductor MPL-AL5030-1R5

EVALUATION BOARD



LxWxH (8.9cmx8.9cmx0.8cm)

Board Number	MPS IC Number
EV2760-VT-00A	MP2760GVT-0000

QUICK START GUIDE

The EV2760-VT-00A evaluation board is designed for the MP2760, a buck-boost NVDC charger, when the device is used to charge a 2-cell battery. The board layout accommodates most commonly used resistors and capacitors. The board's default function is preset for charger mode, and the full charge voltage is preset to 8.4V. In charge mode, the MP2760 can work automatically in buck or buck-boost mode according to the input and battery voltages.

Follow the steps below to prepare the evaluation board.

1. Ensure that the computer has at least one USB port and a USB cable. The MP2760 evaluation software must be properly installed.
2. Connect the USB-to-I^{2}C communication kit (EVKT-USBI2C-02) (see Figure 1).

Figure 1: USB-to-I^{2}C Communication Kit

3. To enable the software, double-click on the “MP2651 Evaluation Kit” .exe file to run the MP2651 evaluation software. The software supports Windows 7 and Windows 10 operating systems.

   The MP2760 evaluation kit.exe file can be downloaded from the MPS website.

Original Test Set-Up for the MP2760

1. Connect the battery terminals to:
   a. Positive (+): VBATT
   b. Negative (-) GND
2. If using a battery simulator, preset the battery voltage between 0V and 8.4V, then turn off the battery voltage.
3. Connect the battery simulator output to the VBATT and GND pins, respectively.
4. Turn on the battery simulator before starting the test.
5. For charge mode testing, connect the input terminals to:
   a. Positive (+): VIN
   b. Negative (-): GND

   Figure 2 on page 4 shows the charge mode testing set-up.

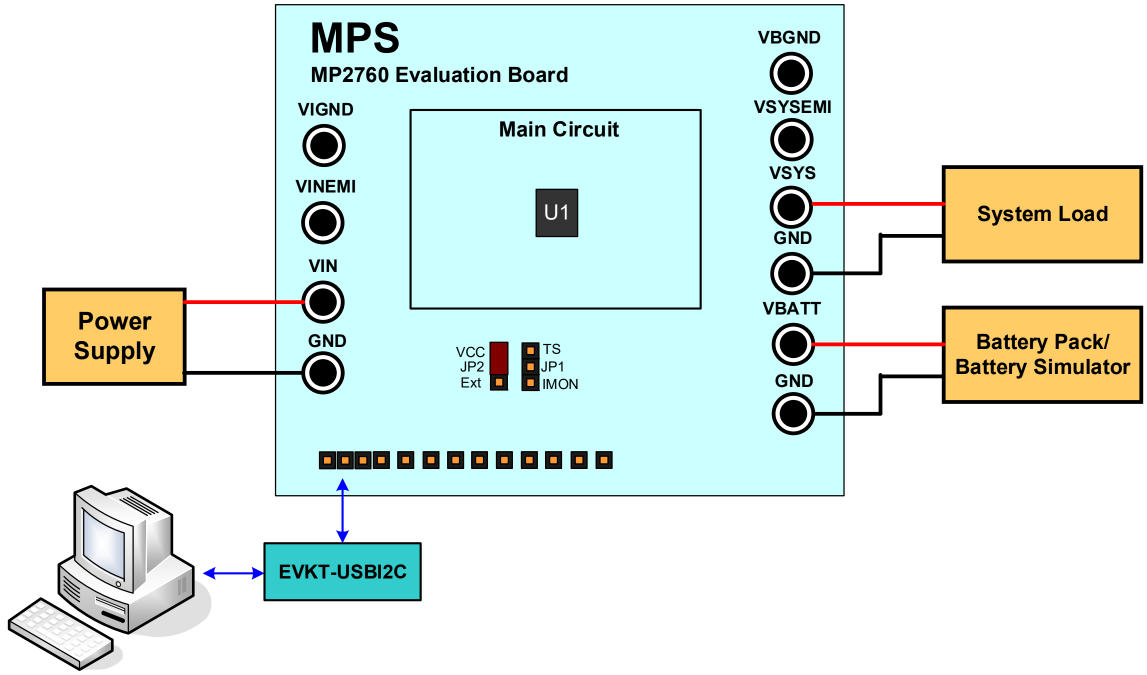


Figure 2: Charge Mode Test Set-Up

6. Connect the system load terminals to:
    a. Positive (+): VSYS
    b. Negative (-): GND
7. For source mode testing, connect the load terminals to:
    a. Positive (+): VIN
    b. Negative (-): GND

    Table 1 shows the jumper connection settings.

Table 1: Jumper Connections

Jack	Description	Default Setting
JP1 (2)	To select the pull-voltage, pull JP1 up to VCC or an external power source.	Pull up JP1 to VCC
JP2 (3)	For the TS/IMON pin's connection, connect TS/IMON to different external circuitry depending on the TS/IMON selection.	Open

Notes:

2) If EXT is selected, add an external power source (e.g. 3.3V) at EXT to AGND. If VCC is selected, no other action is required.
3) TS/IMON has different external circuits. Connect TS/IMON to the corresponding circuit using the I^2C.

8. Launch the MP2760 evaluation software (see Figure 3).

Figure 3: MP2760 Evaluation Software

9. Turn on the input voltage (V_{IN}) to charge the battery and power the system load with the default settings.

Modifying Parameters via the GUI

To use MPS's GUI, ensure that all connections are successful, such as the connections between the computer, USB-to-I²C communication kit, and the evaluation board.

Figure 4 shows the MP2760's basic settings.

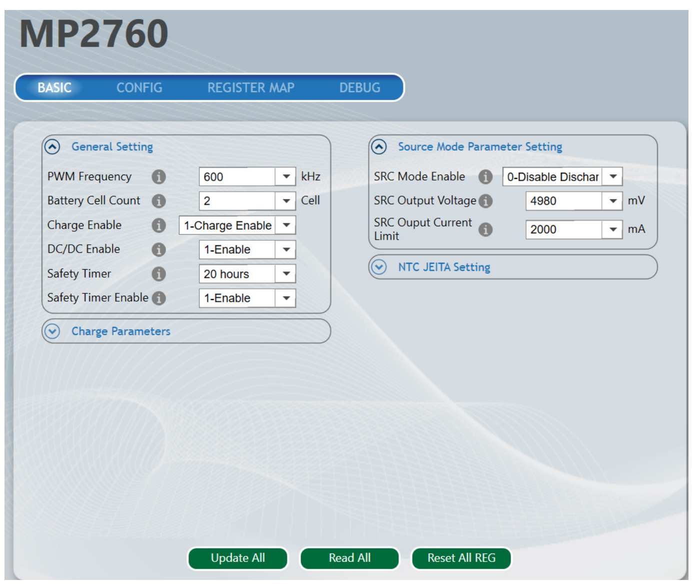


Figure 4: Basic Settings

Figure 5 on page 6 shows how to configure the general settings. These settings include the pulse-width modulation (PWM) frequency, battery cell count, safety timer, basic controls in charge mode (such as enabling the DC/DC converter), and charge enabling.

Note that the recommended PWM frequency is between 500kHz and 800kHz.

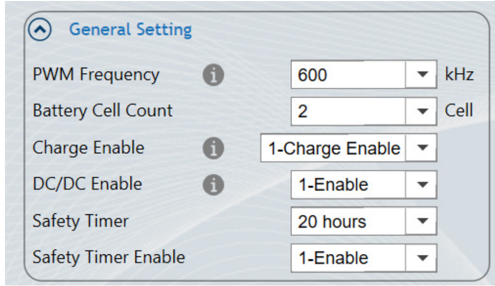


Figure 5: General Settings

Figure 6 shows how to configure the charge parameters, including the battery-full voltage, fast charge current, pre-charge threshold, recharge threshold, trickle charge current, pre-charge current, and termination current.

The charge parameters also provide the parameters for power path management, including the input minimum voltage limit and input current limit. All the parameters can be input directly by keyboard.

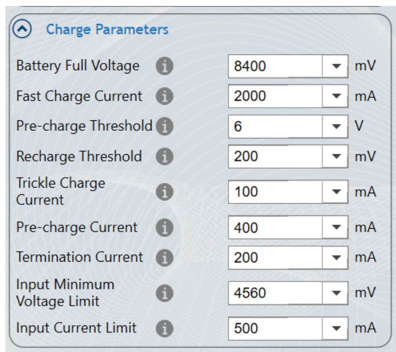


Figure 6: Charge Parameters

Figure 7 shows how to configure the negative temperature coefficient (NTC) JEITA settings for battery thermal protection.

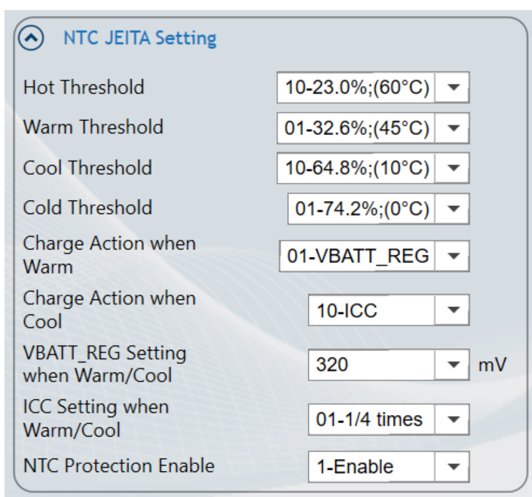


Figure 7: NTC JEITA Settings

Figure 8 on page 7 shows how to configure the source mode settings. In source mode, the battery supplies power to the IN pin. The discharge parameters include the SRC mode (enabled or disabled), SRC output voltage, and SRC output current limit.

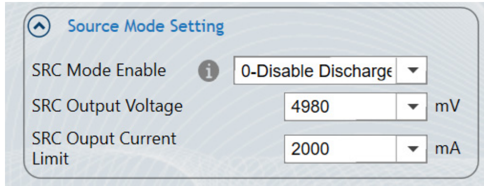


Figure 8: Source Mode Settings

Figure 9 shows the MP2760's configuration settings.

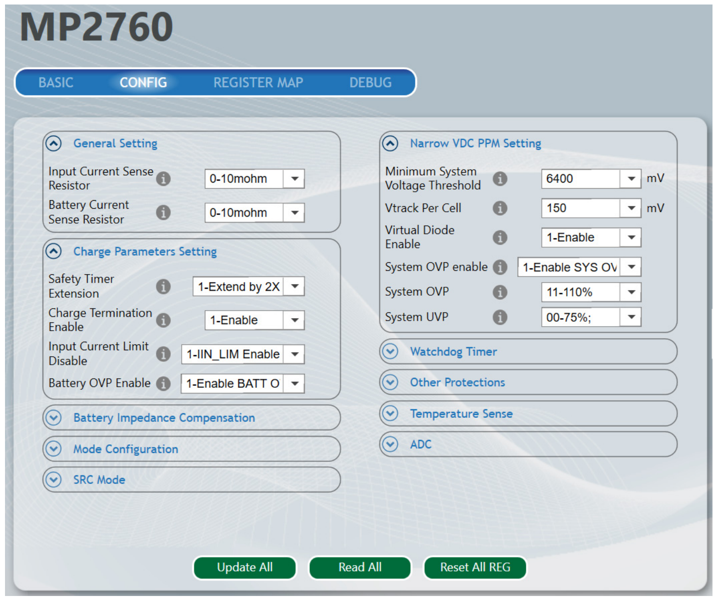


Figure 9: Configuration Settings

Figure 10 shows how to configure and select the current-sense resistors.

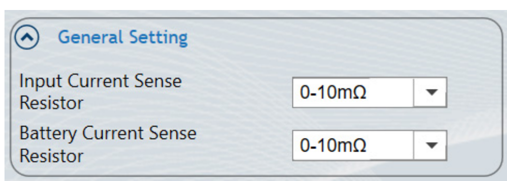


Figure 10: Current-Sense Resistor Settings

Figure 11 shows how to configure the charge protection parameters. These parameters include the safety timer extension, as well as options to enable charge termination, the input current limit, and battery over-voltage protection (OVP).

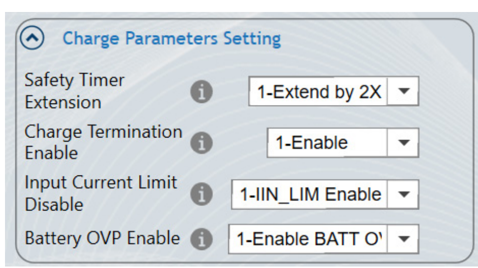


Figure 11: Charge Parameters Setting

Figure 12 on page 8 shows how to configure the battery impedance compensation, including the battery impedance and voltage compensation limit.

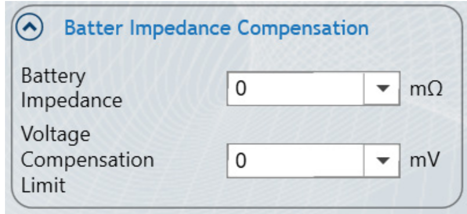


Figure 12: Battery Impedance Compensation

Figure 13 shows how to configure the external MOSFET control. ACGATE can be set to drive the input MOSFET between the ADP pin and the input current-sense resistor. BGATE can be set to control the battery MOSFET between the SYS pin and the battery current-sense resistor.

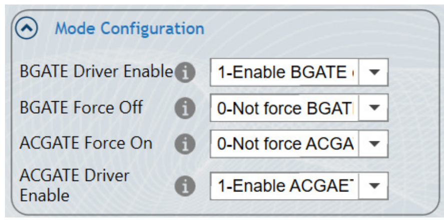


Figure 13: External MOSFET Configuration

Figure 14 shows how to configure the SRC mode control, which includes the SRC output voltage configuration and protections.

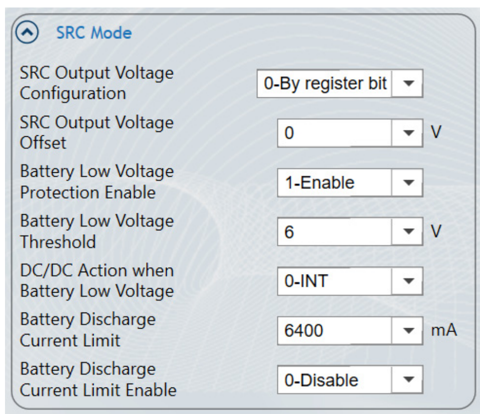


Figure 14: SRC Mode Configuration

Figure 15 shows how to configure the NVDC power path management (PPM).

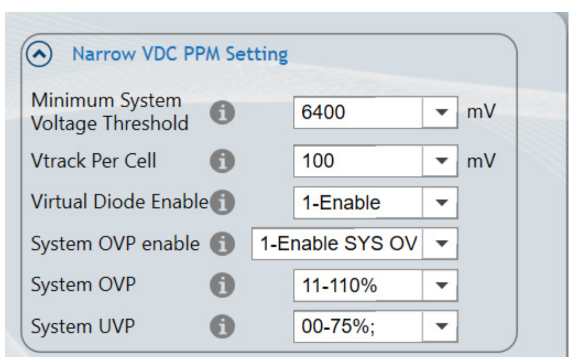


Figure 15: NVDC PPM Settings

Figure 16 on page 9 shows how to configure the watchdog timer.

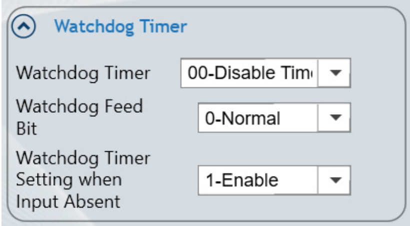


Figure 16: Watchdog Timer

Figure 17 shows how to configure additional protections, including the input under-voltage (UV) threshold, input over-voltage (OV) threshold, and input OV deglitch time.

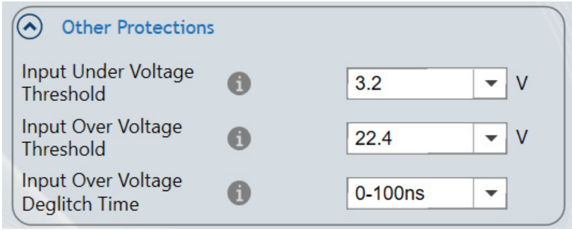


Figure 17: Additional Protections

Figure 18 shows how to configure temperature-sense control. The TS/IMON pin can be set as either the temperature-sense pin (TS) or the battery current monitor pin (IMON).

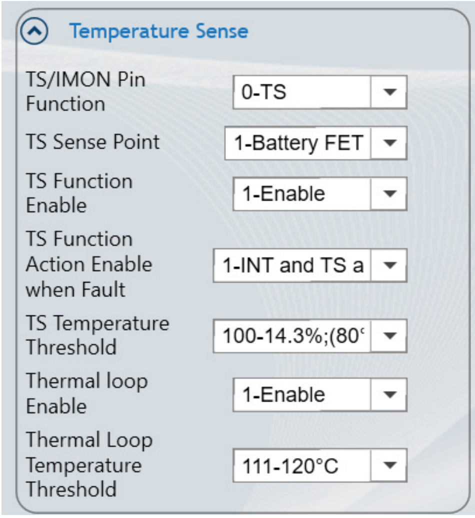


Figure 18: Temperature Sense

Figure 19 shows how to configure the ADC operation mode.

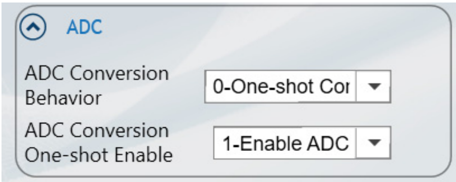


Figure 19: ADC Operation Mode

Figure 20 on page 10 shows the register map, which matches all the register results displayed on the BASIC and CONFIG pages.

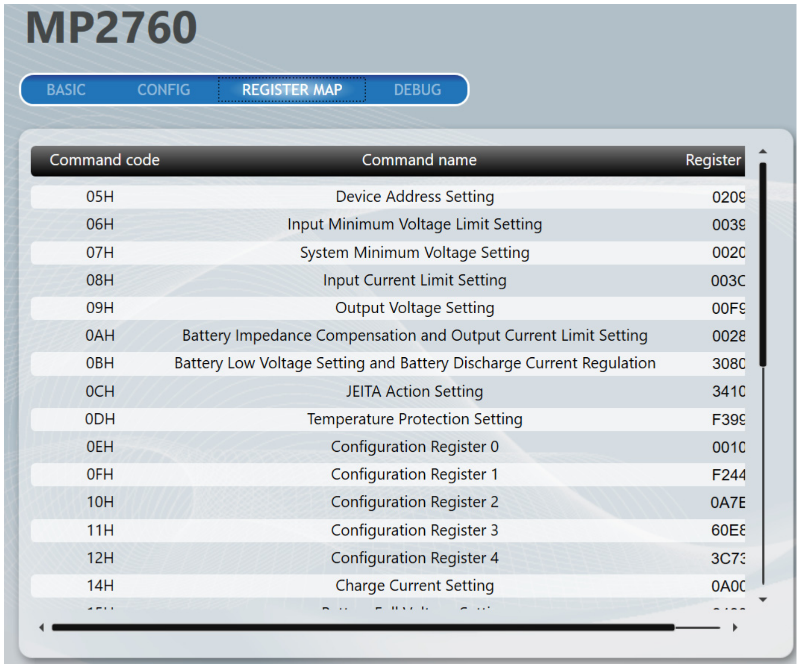


Figure 20: MP2760 Register Map

Figure 21 shows the monitor view.

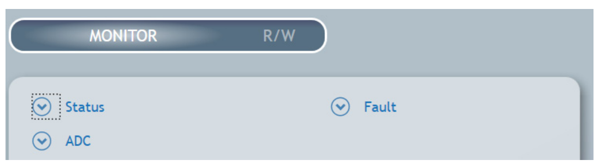


Figure 21: Monitor View

Figure 22 shows how to configure the status.

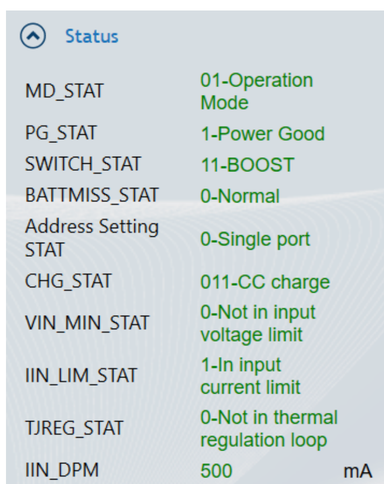


Figure 22: Status Setting

Figure 23 shows how the fault statuses are displayed.

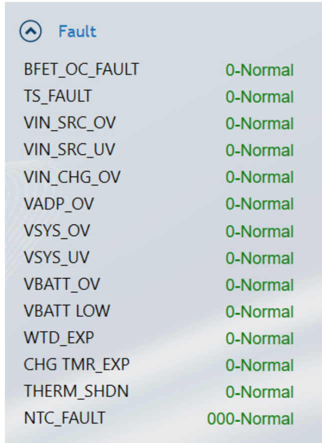


Figure 23: Fault Settings

Figure 24 shows how to configure the analog-to-digital converter (ADC).

Figure 24: ADC Settings

EVALUATION BOARD SCHEMATIC

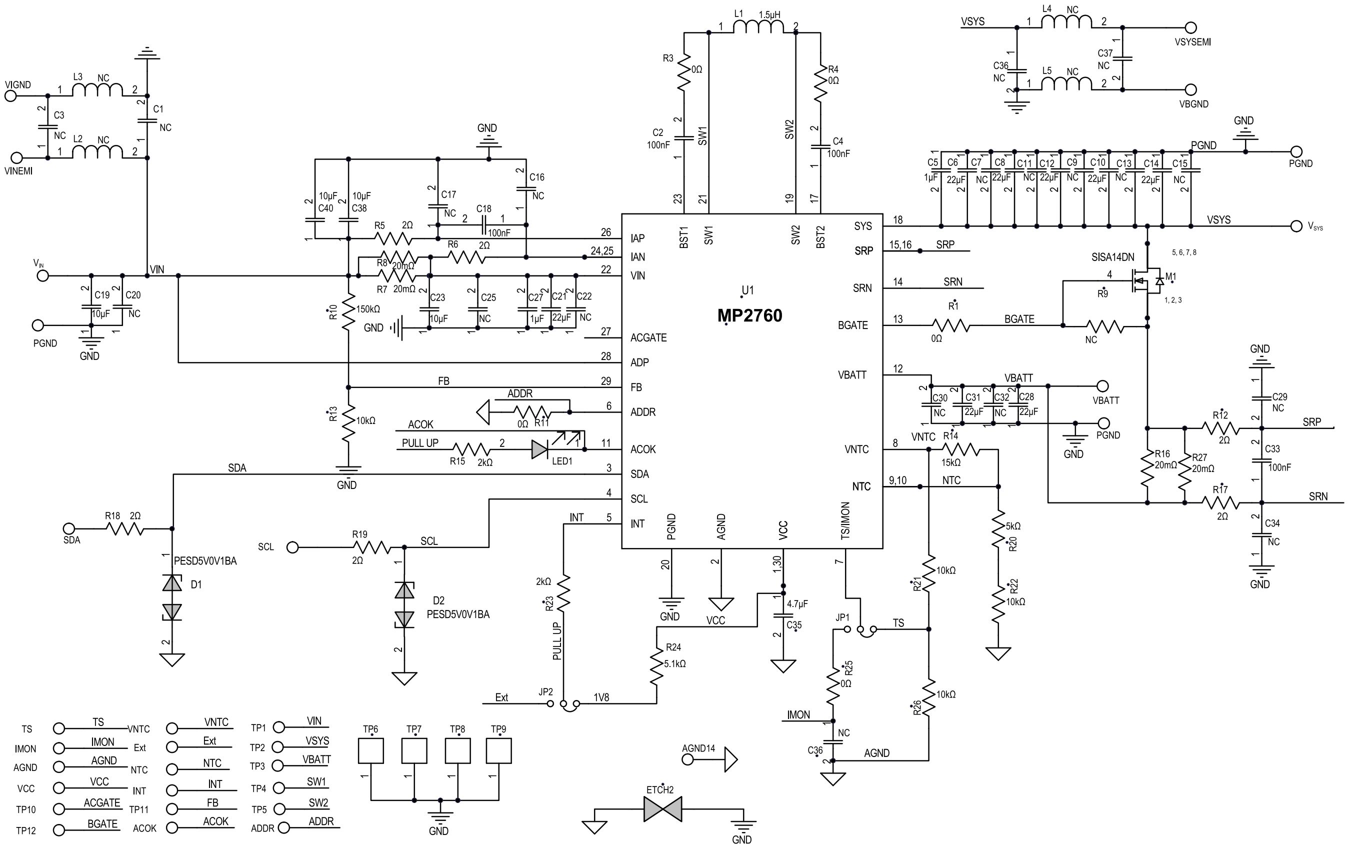


Figure 25: Evaluation Board Schematic

EV2760-VT-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
4	L2, L3, L4, L5	NC				
6	R1, R3, R4, R11, R20, R25	0	Film resistor, 5%	0603	Yageo	RC0603JR-070RL
6	R5, R6, R12, R17, R18, R19	2Ω	Film resistor, 5%	0603	Liz	CR0603JA02R0G
4	R7, R8, R16, R27	20mΩ	Film resistor, 1%, 1/4W	1206	Cyntec	RL1632H-R020-FN
1	R9	1mΩ	Film resistor, 1%	0603	Yageo	RC0603FR-071ML
1	R10	150kΩ	Film resistor, 5%, 1/10W	0603	Yageo	RC0603JR-07150KL
5	R13, R14, R21, R22, R26	10kΩ	Film resistor, 1%, 1/10W	0603	Yageo	RC0603FR-0710KL
2	R15, R23	2kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-072KL
1	R24	5.1kΩ	Film resistor, 5%	0603	Yageo	RC0603JR-075K1L
4	R28, R29, R30, R31	NC				
11	C1, C3, C15, C16, C17, C22, C29, C34, C36, C37, C39	NC				
4	C2, C4, C18, C33	100nF	Ceramic capacitor, 25V, X7R	0603	Wurth	885012206071
2	C5, C27	1μF	Ceramic capacitor, 25V, X5R	0402	Murata	GRM155R61E105KA12
6	C6, C8, C10, C12, C28, C31	22μF	Ceramic capacitor, 25V, X5R	0805	Murata	GRM21BR61E226ME44L
9	C7, C9, C11, C13, C14, C19, C20, C30, C32	NC				
5	C21, C23, C25, C38, C40	10μF	Ceramic capacitor, 25V, X7S	0805	Murata	GRM21BC7E106KE11L
1	C35	4.7μF	Ceramic capacitor, 25V, X5R	0603	Murata	GRM188R61E475KE11D
1	LED1	Red	Red LED	0805	Bright LED	BL-HUE35A-AV-TRB
2	D1, D2	NC				
1	M1	8.5mΩ	N-channel MOSFET, 30V, 20A	PowerPAK 1212-8	Vishay	SISA14DN-T1-GE3
13	ACOK, ADDR, AGND, AGND, EXT, IMON, INT, NTC, TS, VCC, VNTC, SCL, SDA	2.54mm	Pin header	DIP	Any	

EV2760-VT-00A BILL OF MATERIALS *(continued)*

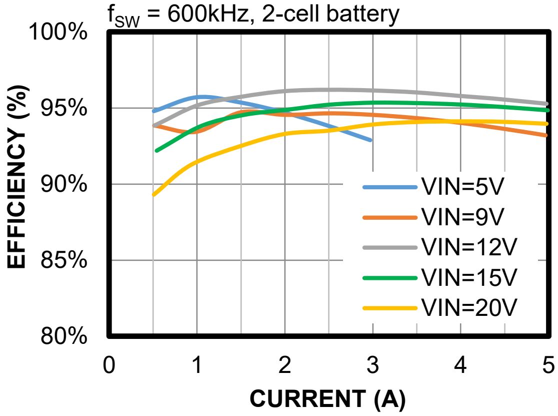
Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
11	TP1, TP2, TP3, TP4, TP5, TP6 (GND), TP7 (GND), TP8 (GND), TP9 (GND), TP11, TP12	1mm	Test point, φ = 1mm	DIP	Any	
10	VIN, VINEMI, VBATT, VSYS, VSYSEMI, GND, GND, GND, VIGND, VBGND	2mm	Test point, φ = 2mm	DIP	Any	
2	JP1, JP2	2.54mm	Pin header	DIP	Any	
1	JP1	2.54mm	Jumper	DIP	Any	
1	L1	1.5μH	Inductor, 9.7mΩ, 9A	SMD	MPS	MPL-AL5030-1R5
1	U1	MP2760	1-cell to 4-cell buck-boost charger	TQFN-30 (4mmx 5mm)	MPS	MP2760GVT-0000

EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. Default setting is for a 2-cell battery, C_{IN} = 10µF x 5 + 1µF x 1, C_{SYS} = 22µF x 4 + 1µF x 1, C_{BATT} = 22µF x 2, L = 1.5µH (10mΩ), f_{SW} = 600kHz, 2-cell battery. T_A = 25°C, unless noted otherwise.

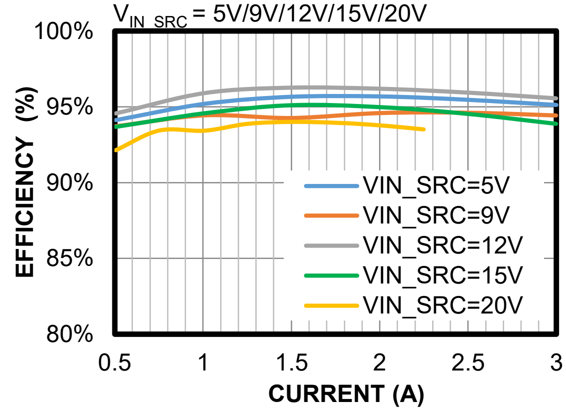
Efficiency vs. Charge Current in Charge Mode

V_{BATT} = 8V, V_{IN} = 5V/9V/12V/15V/20V, f_{SW} = 600kHz, 2-cell battery



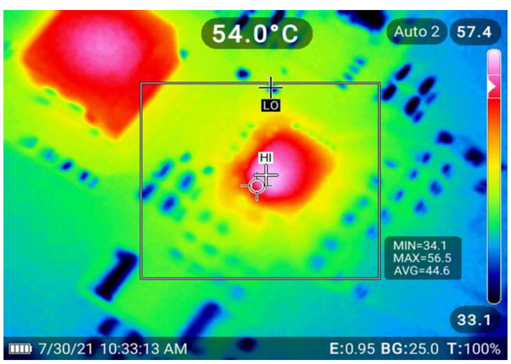
Efficiency vs. Source Current in Source Mode

V_{BATT} = 8.4V, f_{SW} = 600kHz, 2-cell battery, V_{IN_SRC} = 5V/9V/12V/15V/20V



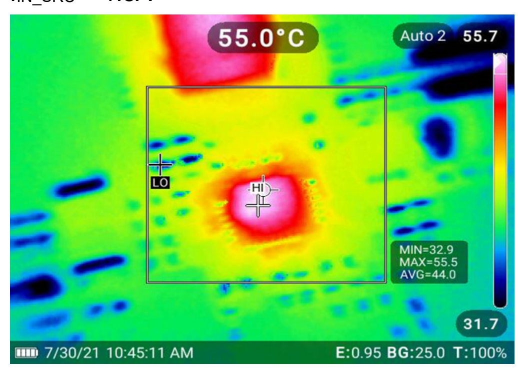
Thermal Performance

Charge mode, V_{IN} = 20V, $I_{INLIMIT}$ = 3A, V_{BATT} = 8.2V, I_{CC} = 5A



Thermal Performance

Source mode, V_{BATT} = 8.4V, V_{IN_SRC} = 20V, I_{IN_SRC} = 1.8A



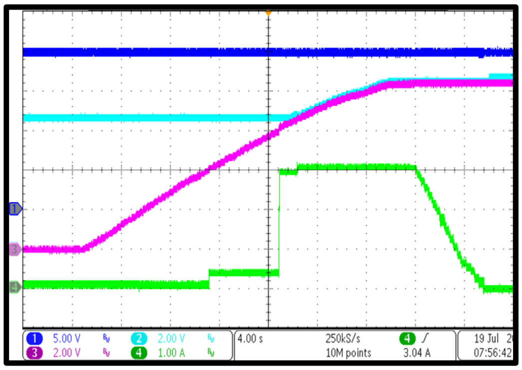
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. Default setting is for a 2-cell battery, C_{IN} = 10µF x 5 + 1µF x 1, C_{SYS} = 22µF x 4 + 1µF x 1, C_{BATT} = 22µF x 2, L = 1.5µH (10mΩ), f_{SW} = 600kHz, 2-cell battery. T_A = 25°C, unless otherwise noted.

Charge Profile Curves

V_{IN_ADP} = 20V, V_{BATT} = 0V to 8.4V, I_{IN_MIN} = 3A, I_{CC} = 2A, V_{SYS_MIN} = 6.4V, V_{TRACK} = 100mV

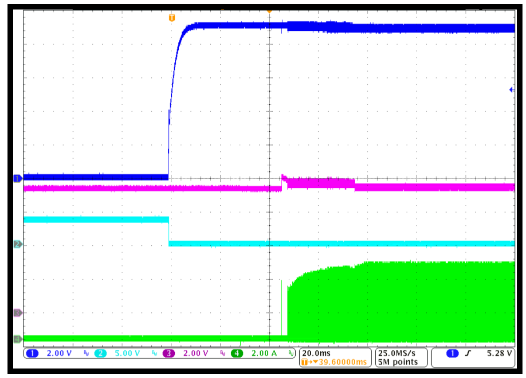
CH2: V_{SYS}
CH1: V_{IN_ADP}
CH3: V_{BATT}
CH4: I_{BATT}



Start-Up through VIN in Charge Mode

9V input power on, V_{BATT} = 7.4V (2 cells), I_{CC} = 2A, charge enabled, I_{SYS} = 0A

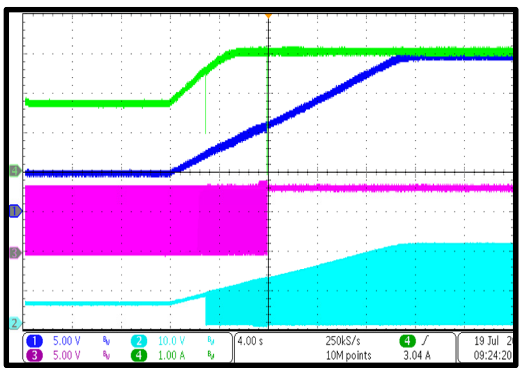
CH1: V_{IN_ADP}
CH2: ACOK
CH3: V_{SYS}
CH4: I_L



V_{IN_ADP} Step from 5V to 20V

I_{IN_MIN} = 3A, V_{BATT} = 8V, I_{CC} = 3A, V_{SYS_MIN} = 6.4V, V_{TRACK} = 100mV

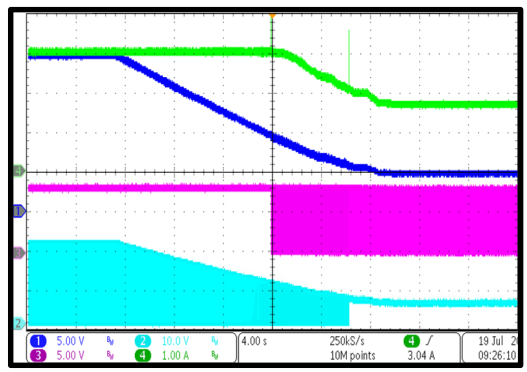
CH4: I_{BATT}
CH1: V_{IN_ADP}
CH3: V_{SW2}
CH2: V_{SW}



V_{IN_ADP} Step from 20V to 5V

I_{IN_MIN} = 3A, V_{BATT} = 8V, I_{CC} = 3A, V_{SYS_MIN} = 6.4V, V_{TRACK} = 100mV

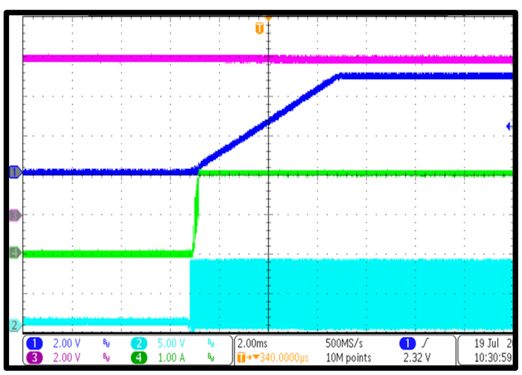
CH4: I_{BATT}
CH1: V_{IN_ADP}
CH3: V_{SW2}
CH2: V_{SW1}



Start-Up through V_{IN_SRC} in Source Mode

V_{BATT} = 8V, V_{IN_SRC} = 5V, I_{IN_SRC} = 2A

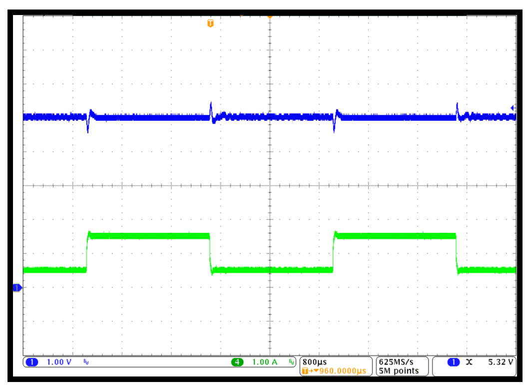
CH1: V_{IN_SRC}
CH3: V_{BATT}
CH4: I_{IN_SRC}
CH2: V_{SW2}



Load Transient in Source Mode

V_{BATT} = 7.4V (2 cells), V_{IN_SRC} = 5V, load current between 0.5A and 1.5A

CH4: I_{IN_OTG}
CH1: V_{IN_OTG}



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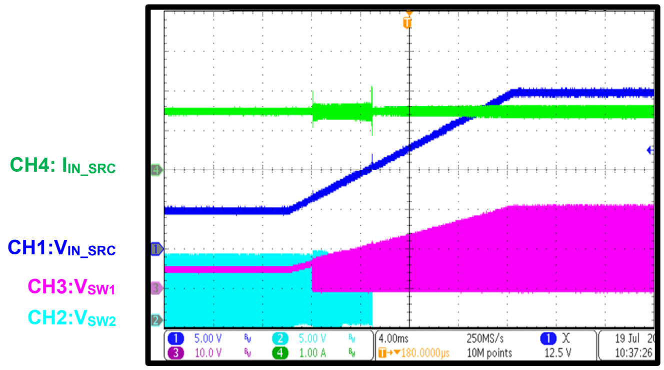
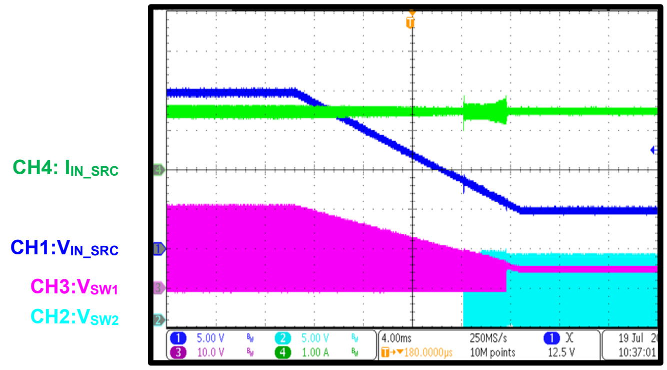
V_{IN_SRC} Step from 5V to 20V in Source Mode

V_{BATT} = 8V, V_{IN_SRC} = 5V to 20V, I_{IN_SRC} = 1.5A



V_{IN_SRC} Step from 20V to 5V in Source Mode

V_{BATT} = 8V, V_{IN_SRC} = 20V to 5V, I_{IN_SRC} = 1.5A



PCB LAYOUT

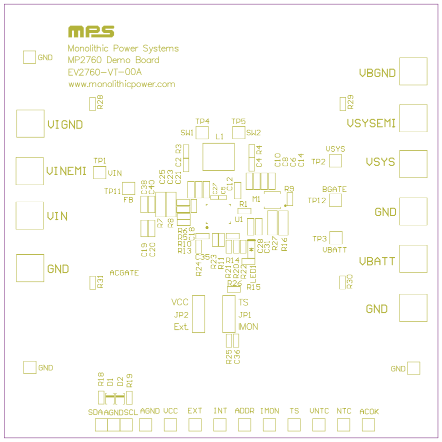


Figure 26: Top Silk

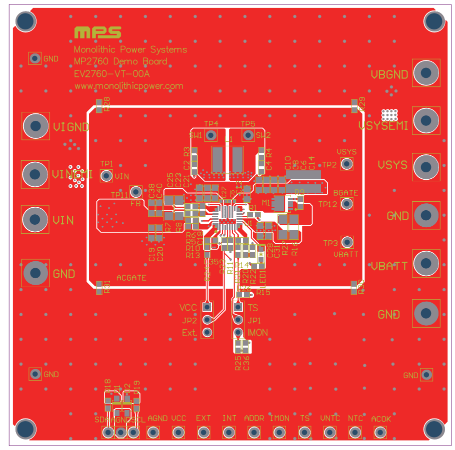


Figure 27: Top Layer

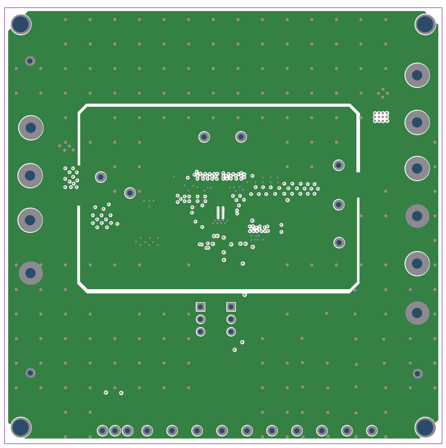


Figure 28: Mid-Layer 1

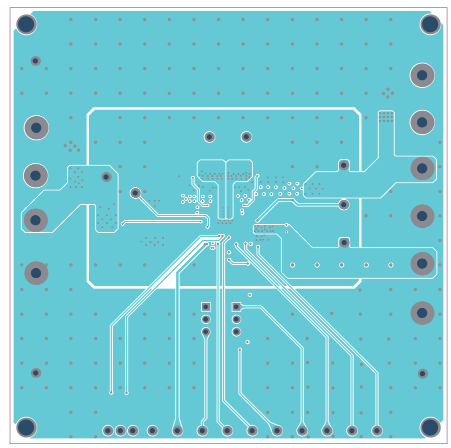


Figure 29: Mid-Layer 2

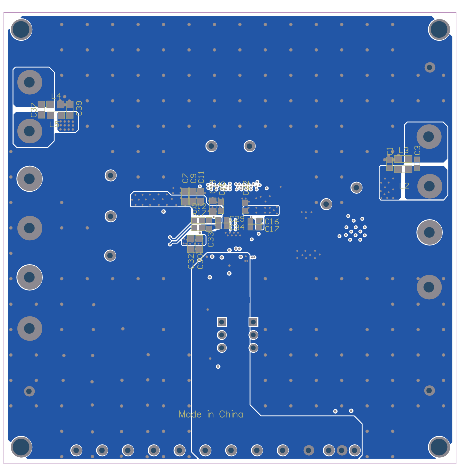


Figure 30: Bottom Layer

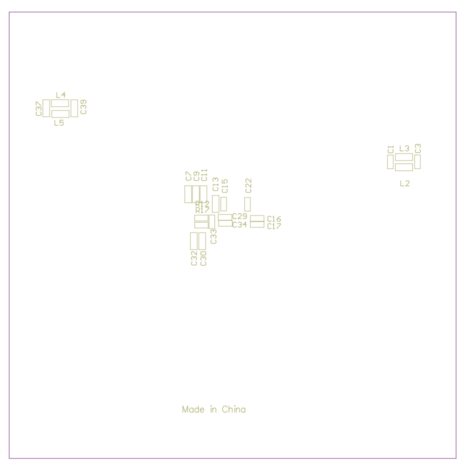


Figure 31: Bottom Silk

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/11/2022	Initial Release	-